Pardeep Garg

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
T-3 EXAMINATION (JUNE 2016)
B.Tech. IVth Semester (ECE)

COURSE CODE: 10B11EC401 MAX. MARKS: 35
COURSE NAME: Digital Electronics
COURSE CREDITS: 04 MAX. TIME: 2 HRS

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means. Attempt all parts of a question at one place.*

Q 1a). Design a sequence detector (using Mealy type FSM) to detect the sequence 1111 which produces an output 1 when the whole sequence is detected. Overlapping is allowed. Design the circuit using D flip flops. Also implement the same using PLA. **(2+2+1 = 5)**

Q 1b). Perform the following operation using BCD subtraction: **735.4 – 68.9** **(2)**

Q 2a). Explain the Astable operating mode of 555 timer. A monostable 555 timer is required to produce a time delay within a circuit, design it to produce a minimum output delay of 600 msec. **(2+2 = 4)**

Q 2b). Design a Mod-14 Asynchronous counter. **(3)**

Q 3a). Design a 4- bit shift register which shifts data in both directions, has parallel loading capability and produces output parallel also **(in one circuit)**. **(4)**

Q 3b). Design a type D counter that goes through states 0, 2, 3, 5, 7, 0….. The undesired states must always go to zero state on the next clock pulse. **(3)**

Q 4a). Draw the circuit diagram of the following logic functions using CMOS logic gate assuming uncomplemented inputs.

i) $\overline{(A + \bar{C}) \times (B + C) \times (\bar{A} + \bar{B})}$

ii) A 2- input XNOR gate **(2+2 = 4)**

Q 4b). Implement 4- bit prime number detector using **one** 4:1 multiplexer. **(3)**

Q 5a). Design a 4-bit BCD to XS-3 code converter using PAL. **(1+2+2 =5)**

Q 5b). Convert $(110110111)_{Gray}$ to 8's complement and Hexadecimal formats. **(1+1 = 2)**