Dr Shruti

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- JUNE 2016

B.Tech VI Semester

COURSE CODE: 10B11EC612 MAX. MARKS: 35

COURSE NAME: VLSI TECHNOLOGY AND APPLICATIONS

COURSE CREDITS: 04 MAX. TIME: 2 HRS

Note: All questions are compulsory.

1. a) Find the midpoint voltage for the circuit shown in Fig 1 **[2.5]**

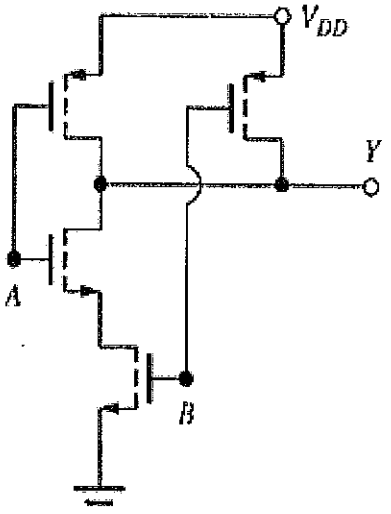

Fig 1

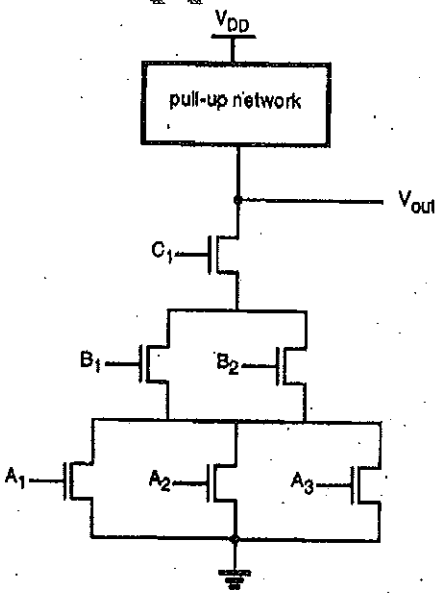

Fig 2

b) A CMOS NOR2 gate is designed using *n*MOS with a value of k_n and *p*MOS by k_p. MOS aspect ratios are 6 and 8 respectively. Find the value of V_{IH} in terms of V_{out} for the case of simultaneous switching if V_{DD} = 3.3V, V_{Tn} = 0.65 V, V_{Tp} = -0.80V, $k`_n$ = 150μA/V$^2$, $k`_p$ = 62 μA/V^2. **[2.5]**

2. Consider the circuit diagram given in Fig 2.

a) Determine the logic function *F*. Find the equivalent *n*MOS inverter circuit for simultaneous switching of all input of Fig 2, assuming that $(W/L)_n = 12$ for all *n*-mos transistor. **[2]**

b) The inverter is biased at 5*V*. The threshold voltages are V_{TOD} = 1V, V_{TOL} = 2V, $K_n`$ = 25μA/V^2 , $\gamma = 0.4V^{1/2}$, $|2\phi_f| = 0.5V$. Design the inverter such that maximum power dissipation is 400μW for output voltage is 0.4*V*. Assume Pull up network as Saturated Load Inverter. **[3]**

3. a) A *p*-channel transistor for which $|V_{th}| = 1.2V$ and $|V_A| = 40V$ operates in saturation with $|V_{GS}| = 2V$ and $|V_{DS}| = 5V$, and $i_D = 5mA$. Find the corresponding signed values for V_{SG}, V_{SD}, λ, k_p` (W/L). **[0.5 + 0.5+ 0.5 + 1 = 2.5]**

   b) A particular enhancement MOSFET for which $V_{th} = 0.8V$ and k_n` (W/L) = $0.1mA/V^2$ is to be operated in the saturation region. If I_d is to be 0.2 mA, find the minimum required V_{DS}. **[1.5]**

   c) For an *n*-mOS transistor for which $V_{th} = 1V$, operating with V_{GS} in the range of 1.25V to 5V, what is the largest value of V_{DS} for which the channel remains continuous? **[1]**

4. In the inverter circuit, what is meant by $Z_{P.U.}$ and $Z_{P.D}$? What are pass transistors? Derive Z_{pu} to Z_{pd} ratio for an *n*MOS inverter driven through one or more series pass transistors. **[1 + 1 + 3 = 5]**

5. Explain the different steps of fabrication of *n* - depletion type IGFET. **[5]**

6. Consider the following parameters for n- channel enhancement type MOSFET having linearly graded junction profile. Substrate doping = 3×10^{12} cm^{-3}, Source/Drain doping = 1×10^{19} cm^{-3}, Sidewall (P+) doping = 2×10^{22} m^{-3}, gate oxide thickness = 40 nm, junction depth= 1.2 μm, length of drain = 10 μm, width = 5 μm, gate drain overlap length= 0.25 μm, $m_{sw} = 0.5$. Both the source and drain diffusion regions are surrounded by P+ channel stop implant. If drain voltage changes from 2.5 V to 5 V, Find drain substrate diffusion capacitance. **[5]**

7. Draw the stick diagram of Sum Function of Full Adder using CMOS logic. **[2 + 3 = 5]**