JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT TEST-3 EXAMINATION -JUNE-2016

B.Tech. II Semester

COURSE CODE: 10B11EC211

MAX MARKS:35

COURSE NAME: BASIC ELECTRONIC DEVICES AND CIRCUITS

COURSE CREDITS:4

MAX TIME: 2HRS

Note: All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.

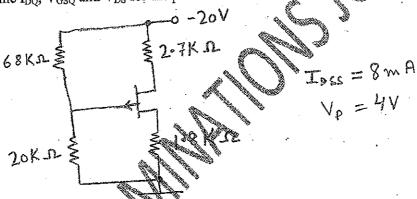
- Q1)
- a) What is the significant difference between the construction of an enhancement -type MOSFET and a depletion-type MOSFET?
- b) In what ways is the construction of a depletion-type MOSFET similar to that of a IFET? In what ways is it different?
- c) Why I_G is effectively zero amperes in enhancement-type MOSFER

(2+3+1=6)

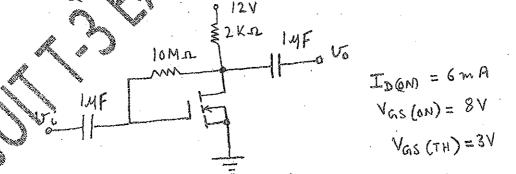
(3)

(4)

Determine $I_{DQ},\,V_{GSQ}$ and V_{DS} for the p-channel JFET Q2)



for the enhancement type MOSFET Determine IDQ and Q3)



Design a voltage-divider bias network using a depletion type MOSFET with I_{DSS} = 10 mA and Q4) V_P =- 4V to have a Q-point at I_{DQ} =2.5mA using a supply of 24V. In addition, set V_G = 4V and use R_D = 2.5 R_S with R1= 22M ohms.

Implement the logic expression f=A.B+C.D using CMOS. Q5)

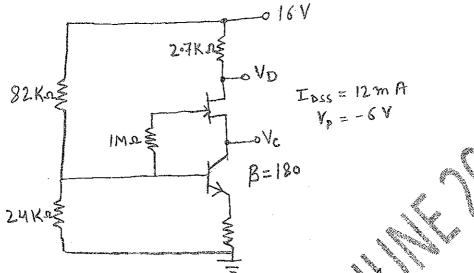
(5)

(4)

(4)

Determine the levels of V_D and V_C for the network. Q6)

(3+3=6)



For the voltage feedback network determine I_C , V_C , V_E and V_C , V_C Q7)



Design a clamper to perform the following function indicated Q8)

