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END SEMESTER EXAMINATION-2015

B.Tech IV Semester

COURSE CODE: 10B22CI421 MAX. MARKS: 45

COURSE NAME: COMPUTER ORGANIZATION

COURSE CREDITS: 4 MAX. TIME: 3 HRS

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

Section A **7*2=14**

All questions carry 2 marks each

1. Explain the concept of delayed branch.
2. What are the different segments of an arithmetic pipeline
3. Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. Find the number of bits needed for cache indexing and the number of tag bits.
4. What is the difference between handshaking and strobe?
5. Give the complete instruction cycle for BSA instruction giving operations performed at different time signals.
6. What are the status bit conditions? Explain with the circuit diagram.
7. What will be the effective address when the addressing mode is relative addressing mode.

Address	Data	
100	Load to AC	Mode
101	Address =400	
102	Next instruction	
324	800	
500	256	
602	451	
800	900	

R1= 324, Base register=100

Section B **4*4=16**

All questions carry 4 marks each

1. Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. What are the number of cache misses for the following sequence of block addresses is 8, 12,0, 12,8

2. Derive the formula for speedup of a pipeline processing over an equivalent non-pipeline processing giving proper diagram of a pipelined system.
3. Differentiate between RISC and CISC.
4. Give the block diagram of a DMA controller. Explain the working of its different parts.

Section C **3*5=15**

All questions carry 5 marks each

1. A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 2 clock cycles for MUL instruction, and 3 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions?

Instruction	Meaning of instruction
I_0 :MUL R_2 ,R_0 ,R_1	$R_2 \leftarrow R_0 * R_1$
I_1 :DIV R_5 ,R_3 ,R_4	$R_5 \leftarrow R_3 / R_4$
I_2 : ADD R_2 ,R_5 ,R_2	$R_2 \leftarrow R_5 + R_2$
I_3 :SUB R_5 ,R_2 ,R_6	$R_5 \leftarrow R_2 - R_6$

2. Consider the following program segment for a hypothetical CPU having three user registers R1,R2 and R3.

Instruction	**Operation**	**Instruction Size(in words)**
MOV R1,5000	R1 <- Memory[5000]	2
MOV R2,R3	R2<- R3	1
ADD R2,R3	R2<- R2+R3	1
MOV 6000,R2	Memory [6000]<- R2	2
HALT	;Machine Halts	1

Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, what will be the return address (in decimal) saved in the stack?

Hint: Byte addressable so 1 word requires 4 bytes.

3. Explain the complete address map for 4 RAMs and 1 ROM. The size of RAM is 128 bits each and ROM 512 bits.