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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

END SEMESTER EXAMINATION-2015

B.Tech VI Semester

COURSE CODE: 10B11CI613 MAX. MARKS: 45

COURSE NAME: Computer Organization and Architecture

COURSE CREDITS: 04 MAX. TIME: 3 HRS

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

Section A **(Marks: 9)**

Justify the following statements with suitable examples, diagram and mathematical formulas.

1. The deep submicron technology will make most of the current IC technologies obsolete.
2. Terahertz Transistor Architecture will allow the continuation of Moore's Law.
3. What is microprogramming?
4. Caches are designed to alleviate this bottleneck by making the data used most often by the CPU instantly available.
5. Why does a computer need so many memory systems?
6. What are virtual and logical addresses?
7. What is the need for reduced instruction chip?
8. Explain the pipeline types.
9. What is programmed I/O?

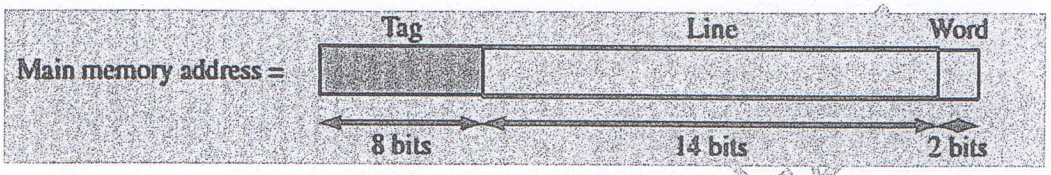
Section B **(Marks: 13.5)**

1. What are the differences among direct mapping, associative mapping, and set-associative mapping? For a set-associative cache, a main memory address is viewed as consisting of three fields. List and define the three fields with diagram. **(4.5)**
2. For the 8-bit word 00111001, the check bits stored with it would be 0111. Suppose when the word is read from memory, the check bits are calculated to be 1101. What is the data word that was read from memory? **(4.5)**
3. What is addressing mode explain the various types of addressing modes with diagrams. **(4.5)**

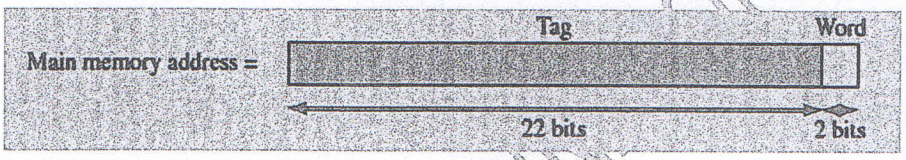
Section C (Marks: 22.5)

1. For the hexadecimal main memory addresses 111111, DDDDDD, BBBBBB, show the following information, in hexadecimal format:

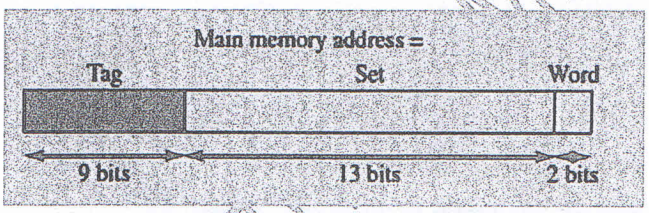
a.



b.



c. .



(4.5)

2. List and briefly define three techniques for performing I/O. Explain the working of 8255 in input/output mode and BSR mode with control word and complete schematic. (4.5)
3. Explain the Booth algorithm in steps while multiplying 2 with -4. (4.5)
4. List and briefly define three types of superscalar instruction issue policies. (4.5)
5. The 5 stages of the processor have the following latencies: (4.5)

	Fetch	Decode	Execute	Memory	Write back
a.	300ps	400ps	350ps	550ns	100ns
b.	200ps	150ps	100ps	190ns	140ns

Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between pipeline stages.

i. Non-pipelined processor: what is the cycle time? What is the latency of an instruction? What is the throughput?

ii. Pipelined processor: What is the cycle time? What is the latency of an instruction? What is the throughput?