

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

MID SEMESTER EXAMINATION-2015

B.Tech VI Semester

COURSE CODE: 10B11CI613

MAX. MARKS: 30

COURSE NAME: Computer Organization and Architecture

COURSE CREDITS: 04

MAX. TIME: 2 HRS

Note: All questions are compulsory. Vague Answers will credit to zero marks

Section A**(Marks: 6)**

Justify the following statements with suitable examples, diagram and mathematical formulas

1. Computer architecture is different from computer organization.
2. Multiprocessing is better than multiprogramming.
3. R-C delay decreases the performance of contemporary computers.
4. Hardwired control logic is faster than micro programmed control logic.
5. Declaration of storage classes of variables in higher level programming languages is dependent upon the instruction set architecture of the underlying processor.
6. Scale out approach for processor design is better than scale up approach.

Section B**(Marks: 9)**

1. Derive the mathematical expression for speed up that can be achieved using n processor system instead of a uniprocessor system. What is law of diminishing returns in multi core systems? [3]
2. Let us assume that the processor is going to execute ADD B, A instruction of 16 bit which stores the sum of the contents of memory locations B and A into memory location A. Partial list of opcodes is 0001: Load AC from memory, 0010:Store AC to memory, 0101: Add to AC from memory. PC content is initialized to 300. Memory snapshot is shown as

Memory Locations	Instructions (Integer Format)
300	1 9 4 0
301	5 9 4 1
302	5 9 4 2
303	2 9 4 2
.....
940	0 0 0 3
941	0 0 0 2
942	0 0 0 4

Show step by step execution of the above said instructions using IR, PC, AC and memory locations. [3]

3. Design traditional bus architecture for your computer. Show all components that you can connect within your bus design. What problems you observe in your design as far as contemporary computers are concerned? Modify your design so as it can fulfill the needs of contemporary computers. [3]

PTO.

Section C

(Marks: 15)

- Imagine that you are the lead architect on a team assigned to design a new multiprocessor computer. The goal for this new product is for it to be a cost performance leader within the server computing market. The marketing team has already specified that the total cost of the machine must fall somewhere within the range of the \$50,000 - \$100,000 that is typical of high-end server machines, and that furthermore it ought to be as close as possible to the low end of this range, so as to best attract the value-seeking customer. You expect that the purchasers in the market for this particular product will not care very much about power consumption, as long as it is less than about 50 kW.

You are trying to choose between two different types of processors to base your system design on. Chip A costs \$2,750, performs at a throughput level of 80 work units (database transactions) per second in a benchmark application, and consumes 100W of power. Chip B costs \$1,600, completes 50 work units per second, and consumes 50W of power. (For this problem, neglect the cost and power consumed by other components.)

In the following, use these variables:

$C_{sys,min}$ = The minimum cost of the system, $C_{sys,max}$ = The maximum cost of the system, $P_{sys,max}$ = The maximum power consumption of the system, C_X = Cost of a chip of type X (where X = A or B) (And similarly with P (power) and T (throughput) of chips A and B), n_{chips} = Number of chips of the selected type in the system.

(a) Identify the design constraints that our system design must satisfy. Also, assuming that power will not end up being the limiting factor in the design, identify the quantities that we should be trying to maximize and/or minimize in this design scenario.

(b) Now, formulate analytical expressions, in terms of the variables given above, for: (i) the constraints that our design must satisfy (ii) the quantity that we should be maximizing in our design (figure of merit) (iii) the quantity that we should be minimizing in our design (figure of demerit)

(c) Answer the following questions and show your work.

(i) Which type of chip (A or B) does a better job of maximizing the figure of merit? (ii) How many copies of this chip should we include in our system design? That is, what is the optimal value of n_{chips} , within the design constraints? (iii) Does the chip that you chose in part (i) also minimize the figure of demerit, within the design constraints?

[7]

- Design typical desktop system PCI configuration and typical server system PCI configuration. Your design should be supported by suitable diagrams showing all the components that can be plugged in such configurations. [4]

- Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

Instruction Type	Instruction Count (millions)	Cycles per Instruction
Machine A		
Arithmetic and logic	8	1
Load and store	4	3
Branch	2	4
Others	4	3
Machine B		
Arithmetic and logic	10	1
Load and store	8	2
Branch	2	4
Others	4	3

- Determine the effective CPI, MIPS rate, and execution time for each machine.

- Comment on the results.

[4]