Prof. Akhil Ranjan

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

END SEMESTER EXAMINATION- May 2015

M.Tech 2nd Sem and B.Tech 8th Sem, ECE

COURSE CODE: 10M21EC211 MAX. MARKS: 45

COURSE NAME: Advanced CMOS Digital Design Techniques

COURSE CREDITS: 03 MAX. TIME: 3 HRS

Note: All questions are compulsory. Marks are indicated against each question.

Section A **(1 x10 = 10 marks)**

1. i> Write two differences between barrel shifter and logarithmic shifter.

ii> Define Carry generate, carry propagate and carry delete. Express sum and carry of a Full adder in terms of these parameters.

iii> Write the logic behind designing carry save multiplier. Compare this with array multiplier.

iv> Write value of propagation delay of 6 bit Ripple carry adder in terms of t_{carry} and t_{sum}.

v> Draw the diagram of implementation of positive latch using transmission gates.

vi> What is Logic restructuring and how it is effective to reduce propagation delay of any logic circuit.

vii> Define the term branching effort with the help of an example.

viii> Draw and explain the circuit of And/Nand gate pair using differential pass transistor logic.

ix> Derive the formula of Dynamic energy transferred by the power supply in one transition of CMOS inverter and how this energy is getting used during circuit operation.

x> What is the reason behind occurrence of short circuit power dissipation. Show the region on DC Characteristics of CMOS inverter, where this power dissipation takes place.

Section B **(5 x3 = 15 marks)**

2> a> Name different components of power consumption in basic CMOS circuits. Explain in detail, the occurrence of these components during the circuit operation.

b> Explain two different techniques of leakage power optimization with suitable diagrams.

(3+2= 5 Marks)

3> Implement three different circuits, which generates a pulse signal of 7ns duration. Assume propagation delay of a gate = 1ns* no. of inputs. Explain the working of each circuit. (5 Marks)

4> a> Explain how pipelining improves the efficiency of any digital circuit. Take the example of a circuit, which performs the exponential operation of (a+b-c).

b> Define Clock gating. Mention two advantages when this technique is used in CMOS circuits.

(3+2= 5 Marks)

Section C

(20 marks)

5> A 5 bit input has to be divided by 2^{n-1}, where n is between 1 to 3. Design a circuit to realize this arithmetic operation. Explain the generalized method how this type of circuit is designed. Explain in detail the operation of your designed circuit. (5 Marks)

6> a> Draw and explain the circuit of Manchester carry chain 4 bit adder using dynamic logic concept. Mention the logic behind design of Manchester carry adder.

b> Draw the circuit of a Schmitt trigger using CMOS and explain its operations. (3+2= 5 Marks)

7>a> Consider a 3 bit gray to binary code conversion circuit. F is the output of a circuit, which will perform the conversion of gray code to binary code for the least significant bit. Design F and F' using Differential Pass Transistor logic.

b> Implement the expression of output carry of Full adder using Differential Cascode Voltage Switch Logic.

(4+2= 6 Marks)

8>a> Write the algorithm which implements register based right shift multiplier network. Draw the circuit which implements this algorithm and explain its operation.

b> Implement Sum and carry of a Full adder using Multiplexer and Transmission Gates.

(2+2= 4 Marks)

********** The End **********