Pankaj Kr

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2021

B.Tech Vth Semester

COURSE CODE: 20B1WEC531 MAX. MARKS: 35

COURSE NAME: Switching Theory and Logic Design

COURSE CREDITS: 3 MAX. TIME: 2 Hours

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

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1. Design an asynchronous negative edge triggered T-Flip Flop. Specify its total state, Primitive flow Table, Merger Diagram. Use SR-NAND Latch for realization of the digital circuit. [7]
2. Implement the Boolean Function $A(x,y,z) = \sum(1,2,4,6)$, $B(x,y,z) = \sum(0,1,6,7)$, using PAL, PLA and PROM. [3]
3. Design a synchronous MOD-12 counter and draw its state diagram also. If two such stages of counter is cascaded and a clock signal of 144 MHz is given as an input. What will be total MOD count and frequency of output signal? [5]
4. Implement $F(A,B,C,D) = \sum(0,2,5,7,11,14)$ using 8 x 1 Multiplexer and use A, B, D as select lines where A is MSB and C is LSB. [5]
5. Write Verilog HDL dataflow and Gate level description of digital circuit.$X = (B + C)(A' + D)B', Y = (B'C + ABC + BC')(A + D'), Z = C(AD + B) + BA'$ [5]
6. According to the transition table in Fig.1, determine all the Race conditions and identify whether it is critical or Non-Critical race. Draw the sequential circuit and write state equation. [5]
7. What are Hazards and its types? According to given circuit in Fig.2, Which Hazard is present in it. How can you remove it using SR- NAND Latch? [5]

10	00	11	10
01	00	10	10
01	00	11	11
11	00	10	10

Fig.1

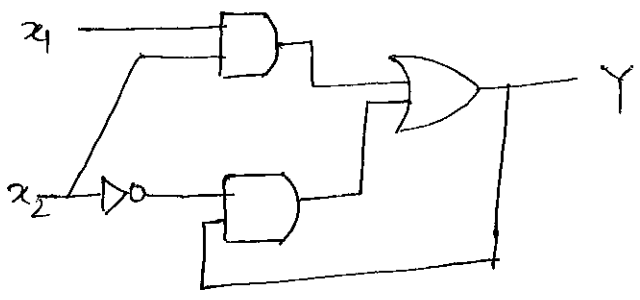

Fig 2.