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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2021

B.Tech. ECE/CSE/IT 3rd Semester

COURSE CODE: 18B11EC312/10B11EC401 MAX. MARKS: 35

COURSE NAME: DIGITAL ELECTRONICS AND LOGIC DESIGN/ DIGITAL ELECTRONICS

COURSE CREDITS: 04 MAX. TIME: 2 Hours

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

1.

i. Write the excitation table for JK flip flop.
ii. Write the characteristic table for T flip flop.
iii. Draw Active high SR latch.
iv. What do you mean by edge triggering? Explain with the help of clock.
v. Which flip flop is used to design Shift registers?
vi. The complemented output of last flip flop is connected to input of first flip flop. Name and draw 2 bit circuit.
vii. Name the sequential circuit given in Figure 1. [7 × 1 = 7]

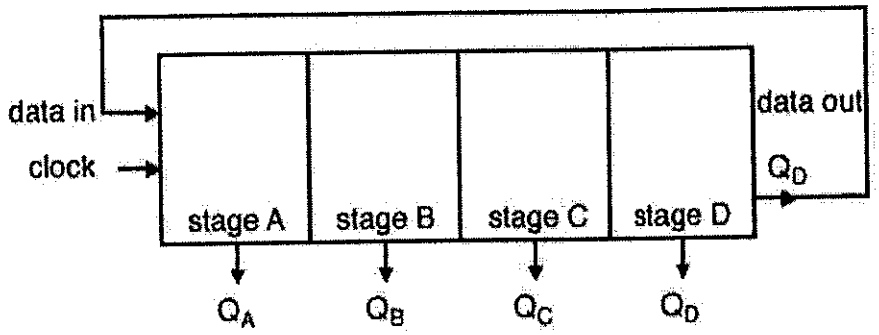

Figure 1

2. Design a circuit for conversion of D to JK flip flop. **[4]**

3. How many flip-flops are required to design MOD-13 up binary counter? Design the circuit in Asynchronous mode with timing diagram. **[5]**

4. Vinay just learned how a three-bit synchronous binary counter works, and he is excited about building his own. He does so, and the circuit works perfectly. Draw the circuit which Vinay has designed assuming T flip flop. **[6]**

5. Design how a shift register circuit could be built from D-type flip-flops with the ability to shift data either to the right or to the left, on command. [6]

6. For the state diagram given in Figure 2, design the sequential circuit using D flip flop.[7]

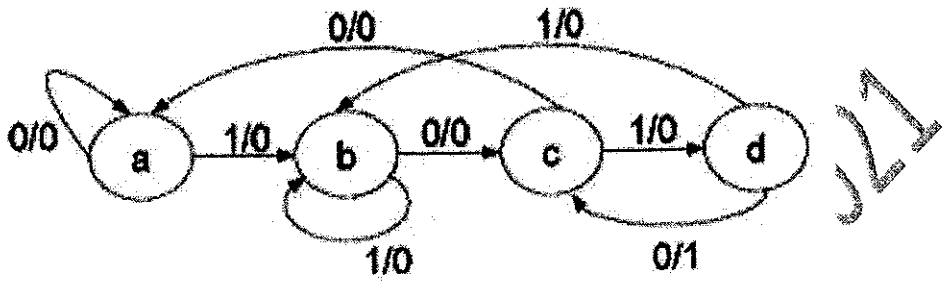

Figure 2