Pradeep Arya

Roll No. .....

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2021

B.Tech. CSE/IT/CE/BT 7th Semester

COURSE CODE: 20B1WEC734 MAX. MARKS: 35

COURSE NAME: DIGITAL SYSTEMS

COURSE CREDITS: 03 MAX. TIME: 2 Hours

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

---

1. Design a sequence detector to detect the binary sequence **1001** using Mealy type FSM with the help of D flip-flops. **[5]**

2. **i)** Obtain the state table, reduced state table, reduced state diagram for the state machine whose state diagram is shown in **Figure 1**. **[1+1+1 = 3]**

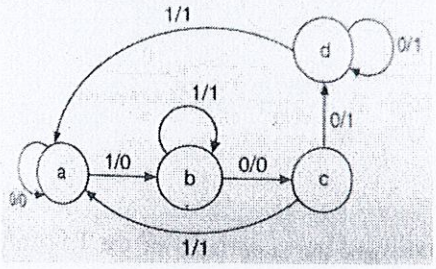

Figure 1

ii) Differentiate between Moore and Mealy type finite state machine (FSM). **[2]**

3. **i)** Design a mod-120 ripple counter using cascading. **[5]**

   ii) A binary ripple counter is required to count up to 4095. How many flip flops are required? If the clock frequency is 9.6 MHZ, what is the frequency at the output of the most significant bit? **[1.5+1.5 =3]**

4. Employing D flip flops; design a 4-bit shift register which has the ability of shifting the data either to the right or to the left, on command. **[5]**

5. Design a synchronous BCD counter using T flip-flops. **[6]**

6. A long sequence of pulses enters a 2-input 2-output synchronous sequential circuit which is required to produce an output z=1, whenever the sequence 1111 occurs. Overlapping sequences are accepted. For example, if the input is 01011111, the required output is 00000011. Draw the state diagram. **[3]**

7. Draw the algorithmic state machine (ASM) chart for the sequence detector to detect the sequence 1011. **[3]**