Dr. Vivek Sehgal

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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- October 2019

M.Tech. I Semester

COURSE CODE: 10M11CI114 MAX. MARKS: 25

COURSE NAME: HIGH PERFORMANCE COMPUTER ARCHITECTURE

COURSE CREDITS: 03 MAX. TIME: 1.5Hr

Note: *All questions are compulsory. Each question carries equal marks. Carrying of mobile phone during examinations will be treated as case of unfair means.*

1. (a) What are the conditions for parallelism? What Quality of Services will improve in computational models for parallel computing and inter-processor communication in parallel architecture?
   (b) Explain the following terms:
   i. Computational granularity.
   ii. Communication latency.
   iii. Flow dependence.
   iv. Anti-dependence.
   v. Output dependence.
   vi. HO dependence.
   vii. Control dependence.
   viii. Resource dependence.
   ix. Bernstein conditions.
   x. Degree of parallelism.

2. (a) Consider the following code fragment:

S1	Load R1, A	R1←Memory(A)
S2	Add R2, R1	R2←R1+R2
S3	Move R1, R3	R1←R3
S4	Store B, R1	Memory(B)←R1

And code fragment involving I/O operations:

S1	Read (4), A(I)	Read array A from file 4
S2	Process	Process the data
S3	Write (4), B(I)	Write array B into file 4
S4	Close (4)	Close file 4

Draw the dependence graph and I/O dependence caused by accessing the same file by read and write statements.

(b) Draw dependence graph showing both data dependence (solid arrows) and resource dependence (Dashed arrows) for following five statements labeled P_1, P_2, P_3, P_4, and P_5, in program order

$$\begin{aligned} P_1&: C = D \times E \\ P_2&: M = G + C \\ P_3&: A = B + C \\ P_4&: C = L + M \\ P_5&: F = G + E \end{aligned}$$

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3. Calculate the grain size and communication latency for multiplying two matrices of size 2X2

$$\begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \times \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix}$$

The assembly code is written in M6800 processor at 20 MHz cycle

   i. Draw the fine grain program graph
   ii. Draw the sequential vs parallel scheduling

4. (a) What is the role of system interconnect architecture in high performance computing? Define the following terms in interconnection networks:
   i. Node Degree and Network Diameter
   ii. Bisection Width
   iii. Data Routing Functions
   iv. Permutations

   (b) What is the difference between perfect shuffle and exchange? Explain with figure

5. (a) List all the Quality of Services for Network Performance
   (b) Explain the following static connection networks:
   i. Ring and Chordal Ring
   ii. Barrel Shifter
   iii. Binary Fat Tree
   iv. Mesh and Torus networks