Dr Vivek

Roll No:.....

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- December 2019

M.Tech. I Semester

COURSE CODE: 10M11CI114 MAX. MARKS: 35

COURSE NAME: HIGH PERFORMANCE COMPUTER ARCHITECTURE

COURSE CREDITS: 03 MAX. TIME: 2Hr

***Note:** All questions are compulsory. Each question carries equal marks. Carrying of mobile phone during examinations will be treated as case of unfair means.*

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1. (a) Write a tabular Summary of static Network for: Linear Array, Ring, Completely Connected, Binary Tree, Star, 2D-Mesh, Illiac Mesh, 2D-Torus, Hypercube, CCC, k—ary n-cube

   (b) Explain the following Performance Metrics and Measures:
   - i. Parallelism Profile in Programs
     - a. Average Parallelism
     - b. Asymptotic Speedup
   - ii. Mean Performance
     - a. Arithmetic Mean Performance
     - b. Harmonic Mean Speedup

2. (a) Explain the following for Design Space of Processors:
   - i. Instruction pipeline Cycle
   - ii. Instruction issue latency
   - iii. Instruction issue rate
   - iv. Simple operation latency
   - v. Resource Conflicts

   (b) What is Instruction-Set Architecture? Explain it for CISC and RISC architectures with architectural distinctions.

3. Explain the following processor architectures with their block diagrams:
   - i. A typical superscalar RISC processor architecture consisting of an integer unit and a floating-point unit.
   - ii. A typical 'VLIW' processor with degree m=3 with 'VLIW' execution with degree m=3

4. (a) Explain the following memory hierarchy properties:
   - i. Inclusion
   - ii. Coherence
   - iii. Locality

(b) What is the use of Virtual Memory? Explain the following for Virtual Memory Models:

i. Address Space
ii. Address Mapping
iii. Private Virtual Memory
iv. Shared Virtual Memory

5. Write a short note on:
   i. Design requirements set by the [EEE 89t.l-I99] Standards Committee for bus design
   ii. Cache addressing Models
   iii. Direct Mapping and Associative Caches