Drain Current and Switching Speed of the Double-Pole Four-Throw RF CMOS Switch

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***Abstract* – Established RF CMOS switch contains MOSFET in its main architecture with a 5.0 V of control voltage and required high value of resistance in circuitry of transceivers to detect the signal. To avoid the high value of control voltage and those resistances, we proposed a Double-Pole Four-Throw switch using RF CMOS technology and verified its performance interns of currents and switching speed. Also to provide a plurality of such switches, where the power and area could be reduced as compared to already existing transceiver switch configuration, which is simply a reduction of signal strength during transmission for RF. Our result shows that the peak output currents in these devices are around 0.387 mA and the switching speed is 30 - 31 ps.**

Keywords – CMOS Switch; DP4T Switch; Drain current; Radio Frequency; RF Switch; Switching Speed; VLSI.

I. INTRODUCTION

The outstanding improvement in the frequency response of Silicon CMOS devices in recent years has motivated their use in millimeter-wave applications as the millimeter-wave regime includes high capacity wireless in local area network, wireless personal area networks, and collision avoidance radar for automobile and civil aviation. Higher levels of integration and lower cost can be achieved with silicon CMOS for these applications, also improving the efficiency. As for the last decades the single-gate MOSFET in planar integrated CMOS technology dominated the semiconductor industry. Enormous progress has been made to scale transistors to ever smaller dimensions to obtain faster transistors [1], as well as to lower the effective costs per transistor in terms of transistors per area. With scaling device dimensions and increasing short channel effects, multiple gate transistors have been investigated to obtain an improved gate control [2, 3].

In the aforementioned radio transceiver systems, to improve the transmission capability and reliability, multiple antenna array system is used. With the multiple antenna arrays, data transfer rate can be increased by the same factor as the number of antenna used. An antenna selection system and RF switch is essential to avoid the uses of multiple RF chains which are coupled with the multiple antennas. The desired switching system must have a simple and low cost structure, which also confine all the improvement of Multiple-Input, Multiple-Output (MIMO) systems. For this purpose we present a comprehensive design of the RF switch with respect to drain current, switching speed and the voltages with the new proposed model for Double-Pole Four-Throw (DP4T) switches. Device structures with layout and widths are studied to understand the effect of device geometry on RF CMOS. This proposed switch is low in cost and capable of selecting data streams to or from the two antennas for transmitting or receiving processes, respectively [4].

For the purpose of designing a DP4T RF CMOS switch, we organize this paper as follows. The basic concept of transceiver switch and the proposed DP4T RF CMOS switch are described in the Section 2. The logic circuit design of transceiver switch with help of layout for DP4T along with simulated current is discussed in the Section 3. The switching speed is analyzed in the Section 4 and at last the Section 5 concludes the work.

II. DP4T RF CMOS TRANSCEIVER SWITCH

Since the modulated signal is transmitted through a switch and the switch makes its way to the antenna for releasing into space. This modulated signal is received by the antenna and makes its way through the switching path to the receiver. A Single-Pole Double-Throw (SPDT) is the fundamental switch that links between one antenna and the transmitter/receiver. A symmetric Double-Gate (DG) MOSFET results when two gates have the same work function and a single input voltage is applied to both gates. An asymmetric DG MOSFET either has synchronized but different input voltages to two identical gates, or has the same input voltage to two gates that have distinct work functions [5]. To avoid the application of these two gate and respective voltages, we proposed a DP4T RF CMOS switch.

Due to the single operating frequency, SPDT switch has a limited data transfer rate. Therefore, the proposed DP4T switch designed is useful to enhance the switch performance for MIMO applications. This DP4T switch can send and receive two parallel data streams simultaneously [6, 7]. We have designed a DP4T RF CMOS switch with the inverter technology. Its performances, such as drain current, switching speed, and applied voltages are discussed in following sections. The designed DP4T switch using CMOS technology is shown in Fig. 1.

The objective of proposed design of a switch is to operate at from 1 GHz to 60 GHz frequency range for MIMO systems. According to the previous reported literatures [4, 6-8], DP4T

switch is a fundamental switch for MIMO applications because parallel data streams can be transmitted or received simultaneously using the multiple antennas. For instance, the transmitted signal from power amplifier is sent to the transmitter 'A' which is shown in Fig. 1 with named as 'A_T_x' port and travel to the ANT_1 node while the received signal will travel from the ANT_2 node to the receiver 'B' with a named as 'B_R_x' port and pass onto the Low Noise Amplifier (LNA) or any other application. The proposed switch contains CMOS in its architecture and needs only two control lines (V_1, V_2) of 1.2 V to control the signal traffic between two antennas and four ports [9]. In addition, signal fading effects can be reduced because sending identical signals through multiple antennas will most likely result in a high quality combined signal at the receive end.

III. Layout and Current Measurement for DP4T Transceivers Switch

For the purpose of current and switching speed we draw the layout of DP4T transceiver switch as in Fig. 2. This shows the layout of DP4T with two input voltages (V_{in1} and V_{in2}) and output through antennas (ANT_1 and ANT_2) with two transmitters (T_x_A and T_x_B) and two receivers (R_x_A and R_x_B). Fig. 3 shows the antenna voltage V_{out1} and V_{out2}, with input voltage V_{in1} and V_{in2} for DP4T CMOS transceiver switch. Drain current for DP4T transceiver switch with output voltage is shown in Fig. 4, which gives $I_{dd\ (max)}$ 0.387 mA, $I_{dd\ (avg)}$ 0.020 mA also rise time 31 ps for 1 GHz operating frequency.

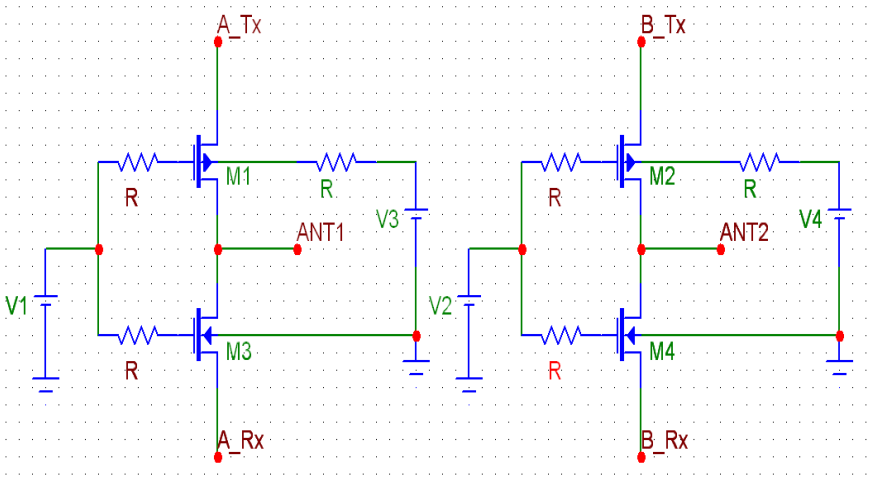
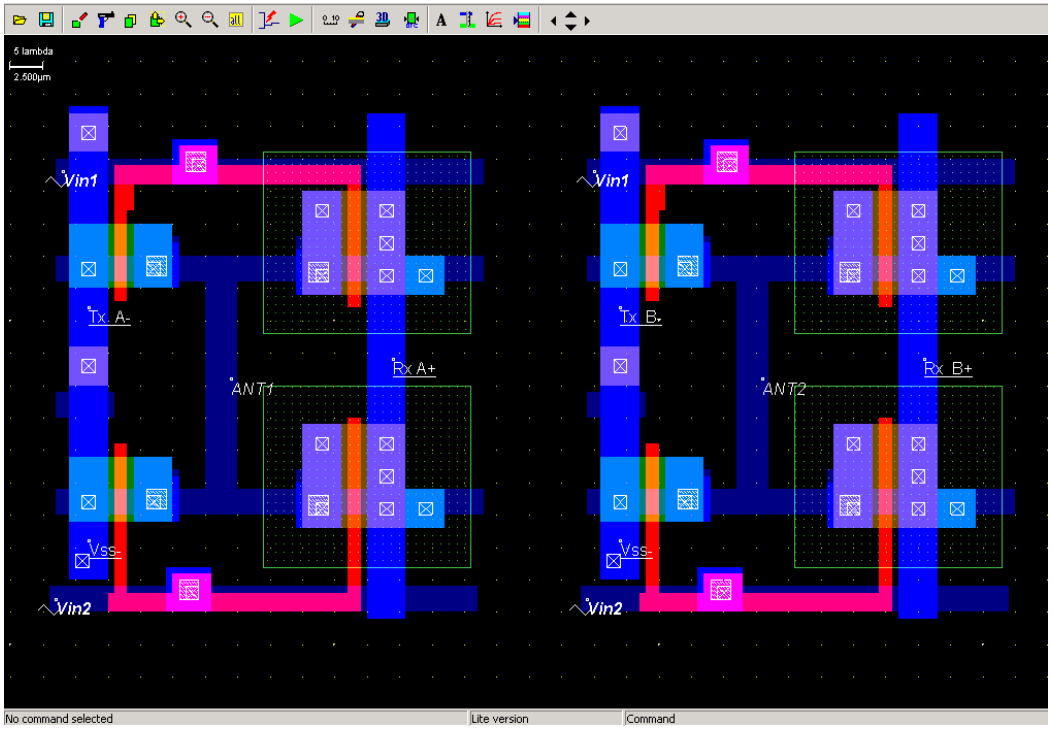


Figure 1. DP4T RF CMOS switch with inverter property.



(a)

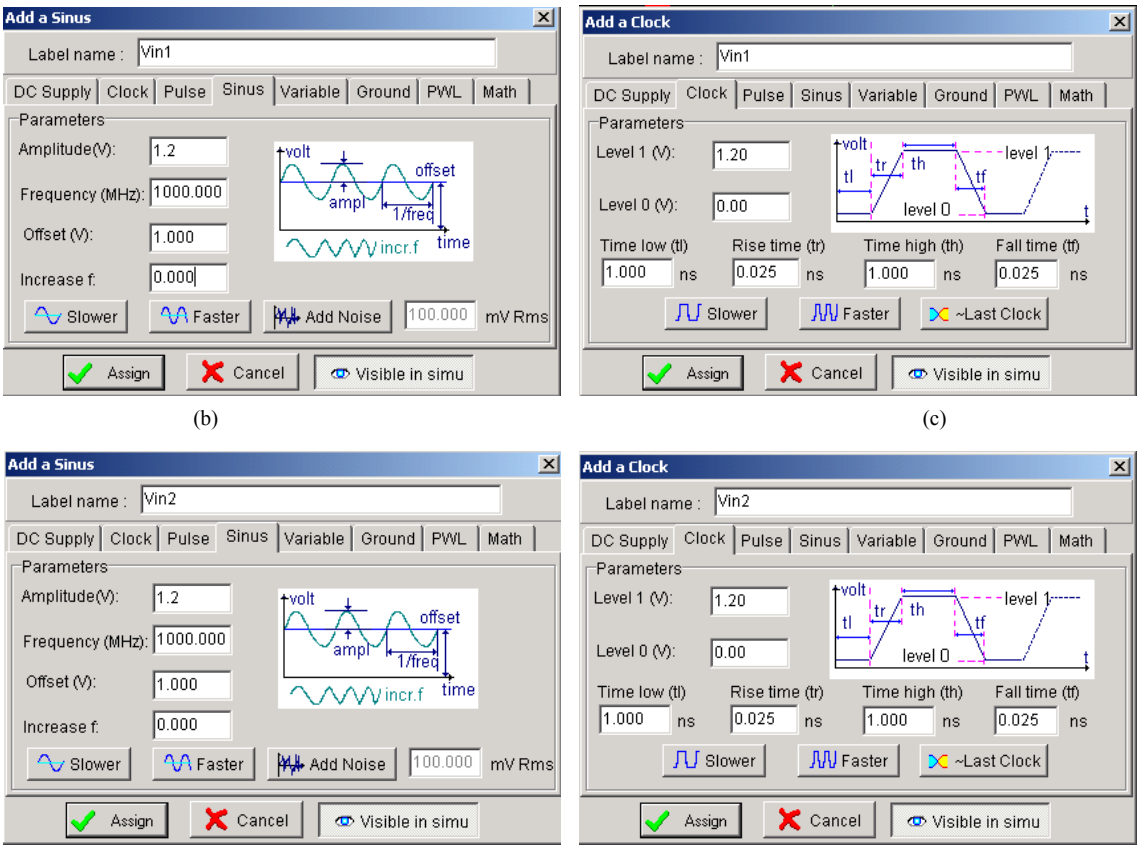


Figure 2. DP4T RF CMOS switch (a) Layout, and (b to e) Applied input voltages.

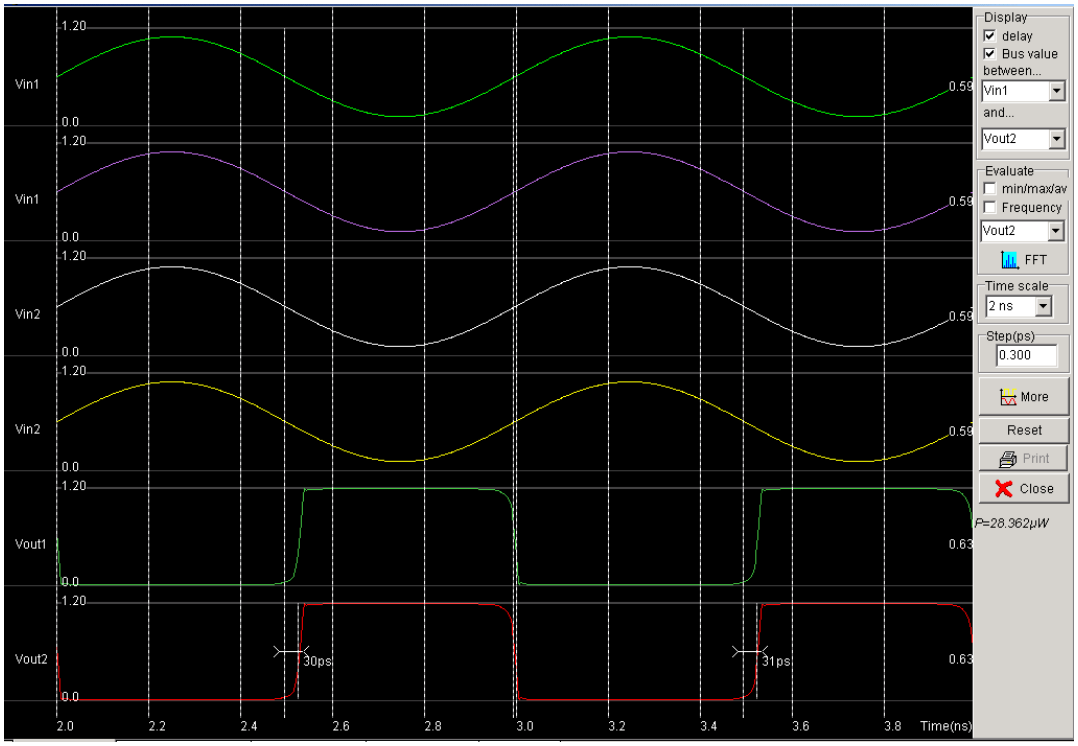


Figure 3. Output Antenna voltages with respect to input voltages for DP4T RF CMOS transceiver switch.

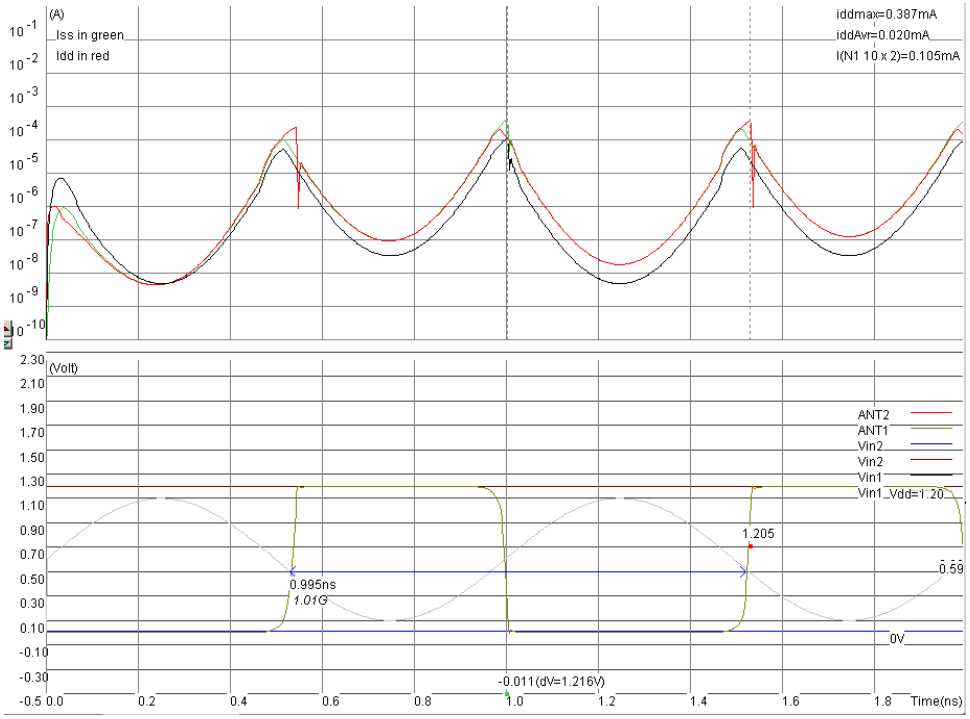


Figure 4. Drain current for DP4T transceiver switch with output voltage.

We also established that for the antenna at the frequency of 1 GHz, maximum data interns of voltage are measured. This data density decreases with the increase in frequency. For example at 0.93 GHz, voltage received by a transceiver system is 313.25 mV and at 8 GHz this is 0.02 mV as shown in Fig. 5. After simulation of DP4T transceiver switches, we found the results for drain current which is shown in Table 1 and we compare their results with the existing models for given references as shown in Table 2.

IV. Switching Speed

The switching speed of the transceiver switch is characterized by the rise time and fall time. Switching speed for the DP4T transceiver switch are summarizes in Table 3. In this simulation, the control voltages are 50 percent of duty pulses with a high level of 1.2 V and a low level of 0 V, the input signal is a sinusoid waveform at 1 GHz. The switching speed is measured as 30 ps to 31 ps during a transmission. This fast switching speed is possible owing to the small switching transistors. This sub-nanosecond switching speed is much faster than the speed of GaAs switch operating at GHz frequencies which is usually on the order of tens of nanoseconds [6]. The switching speed can be improved by decreasing the values of the gate resistors as long as the resistors are still large enough to make the gates open to AC signal.

TABLE I. Simulation Results For Drain Current

Structure	Drain Current
DP4T	0.387 mA

TABLE II. Comparison of Drain Current with Existing Model

References	I_{dd} (mA) at 1 V
[10]	9.80
[11]	5.00
[12]	2.20
[13]	1.75
[5]	1.00
[14]	0.50
This work	0.387

TABLE III. Simulation Results For Switching Speed

Structure	[1]	[15]	[16]	This Work
DP4T	40 ps	400 ps	300-1000 ps	30 ps - 31 ps

The device characteristic including ON and OFF currents can be optimized by the choice of device geometries, aspect ratios, gate material, work-function, threshold voltages etc. Possibility of independent double-gate technologies (four terminal devices) can be of significant advantage for low power and high performance circuit design. The usefulness of the proposed design of DP4T is shown in a class of low power and high performance circuits such as wireless communication system, dynamic logic circuits, Schmitt trigger, SRAM cells, and sense amplifiers.

V. Conclusions

In this paper, the design of a transceiver switch at a low-cost CMOS technology for DP4T has been presented. This switch exhibits good matching with drain current and switching speed. The presented switch is suitable for short

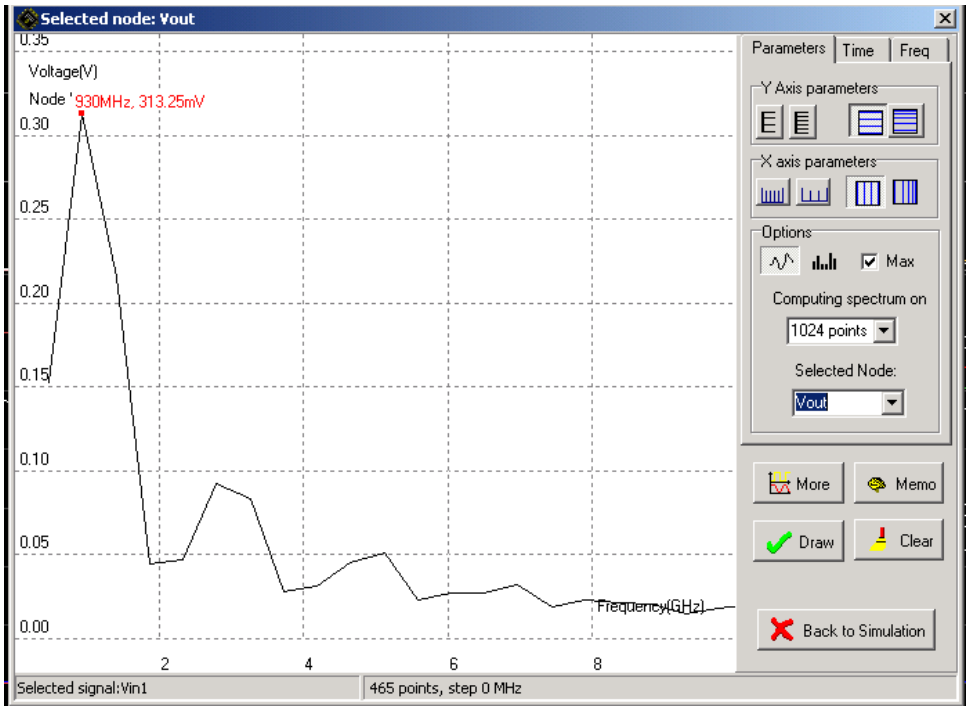


Figure 5. Antenna (ANT_1 and ANT_2) output with different frequencies for DP4T transceiver switch.

range wireless communications where power handling requirements are not very high.

Here we have analyzed the current and switching speed response of DP4T low-power CMOS switches. The proposed device simulation result shows that the peak output currents in these devices are around 0.387 mA and 30 - 31 ps. Based on the simulation results, it is demonstrated that drain currents increases with structures as shown in Fig. 5. Better reduction of the short channel effects and improvement of the device reliability could be expected by changing the length ratio of the gate materials and optimizing them. A device structure with a double gate contact shows a slight improvement in currents and switching speed compared to a single gate contact structure [17, 18]. Since the operating frequencies of the switch are few MHz to 8.0 GHz, it is also useful in wireless local area network and high power RF MOSFET targets VHF applications.

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