PERFORMANCE ASSESSMENT OF DEVICES BEYOND THE SCALING LIMITS– DOUBLE-GATE AND SURROUNDING-GATE MOSFET

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ABSTRACT

Complementary Metal Oxide Semiconductor (CMOS) technology advancement for improving the system reliability, current drive, computational capability and integration density at lower cost has reached to a limit where the significant undesirable effects appear, which further poses tremendous challenges beyond the 45 nm technology node. Therefore, for the further advancement of technology this would also be beneficial for the circuit designers as well as the communication market come with the more innovative device structures. Among which the double-gate MOSFET, due to increase in the mobility, ideal sub-threshold slope, high drain current, reduced power consumption and screening of source end of the channel by the drain electric field, and the surrounding-gate MOSFET, due to increase in gate control and, low-off state current, have emerged as better alternative device structures for the reduced short channel effects and achieving a compact device with a much reduced dimension. In this dissertation, an analytical modeling of both the devices is performed with the help of Poisson equation and gradual channel approximation. Moreover, the expressions are derived using the surface potential model based on drift-diffusion approximation, which is important for the future requirement of the technology. The modeling of terminal charges and trans-capacitances are also presented which are further used for the circuit simulation. Finally, for the small-signal analysis, the trans-capacitances are used to yield the Y-parameters and S-parameters of the device, which would characterize the device for the specified frequency regime of the spectrum for the application as an amplifier and as a switch in the wireless communication transceiver, based on the power gain analysis and on-state switch circuit analysis, respectively. In addition to this, the influence of the Gaussian doping in vertical direction (across the radius) of the surrounding-gate MOSFET on the device performance based on certain assumptions is also presented.

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Himangi Sood

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[1] Himangi Sood, and G. Singh, "A device for ultimate scaling and high frequency-symmetric double-gate MOSFET", International Journal of Electronics and Tele-communication (Under Review), April 2015.

[2] Himangi Sood and G. Singh, "Performance analysis of undoped and Gaussian doped surrounding-gate MOSFET", Journal of Semiconductor (Under Review), May 2015.

CHAPTER 1
INTRODUCTION

Over the last two decades, it is observed that every 18 months the wireless data rate doubles and are approaching the capacity of wired communication systems as can be seen in Fig. 1.1 [1]. In addition to this, till 2020 the data rate is reaching out to be greater than 1 Gbps.

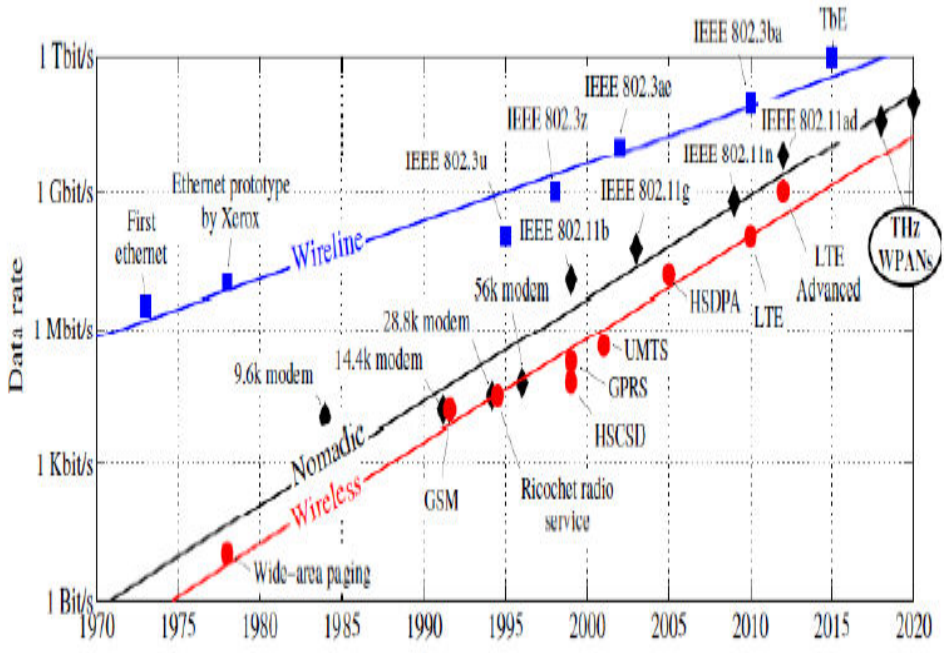


Fig. 1.1 Edholm's law of data rates [1].

Therefore, to meet the requirement for the future wireless network, new technologies are needed which are having high data capacity and reduction in the overall power consumption of the system. Therefore, the THz range of frequency spectrum (from 300 GHz to 3000 GHz) can provide multiple GHz channel bandwidths. This spectrum provides the possibility to transmit at high data rate that is multi-gigabits per second. The recent research activities in THz technologies are increasing into much broader applications such as medical imaging, and wireless sensors and communications [2, 3]. Akyildiz et al [4]

discusses that the THz band communication will be addressing the capacity limitation of the current wireless communication system. Moreover, the other foremost requirements of the next generation communication system are the low power consumption and high processing speed, which should also be met in a much effective way.

In addition to this, the major key for enabling the effective wireless communication, networking is the radio frequency integrated circuits (RFIC). The analog designing and the high frequency designing techniques adds up to form RFIC design. Moreover, the analog designing is used at the low frequencies and the high frequency designing make use of the microwave theory where the concept of the transmission line is very important [5]. In addition to this, the higher frequency RF circuitry can be built by merging various forms of chips together and by using the same process as that for the traditional digital or baseband circuitry, that otherwise would be divided into multi-chip sets. However, single-chip integration also reduces the drawn current by reducing the number of off-chip loads that are necessary to drive multiple, non-integrated chipsets [6]. Moreover, the customer's requirements from RFIC design are the portability, universal, low power, multi-functionality, and miniaturization, which would further combine to reduce the overall cost of the of system on chip.

However, due to the reduced energy consumption of the MOSFET, they are seen to be the better option for ultra-fast communication [7]. Although, the designing of the device for the high frequency range a very crucial task, therefore new device structures are to be incorporated into the communication system that would provide the desired performance in the next generation communication system. However, Fujishima [8] demonstrated how low power and high speed communication for THz can be balanced. In addition to this, MOSFET has been an emerging device for RF/analog applications and the demand of the industry is encouraging for the replacement of the costly, huge sized and more power consuming devices with low power and high-density radio frequency devices.

Before, moving on to the new device structures of MOSFET and the RFIC design performance parameters in the THz range, the next section is going to give a brief idea of MOSFET and tool used for the technology advancement.

1.1. MOSFET

Initially, the need for the smaller, cheaper, faster, less power consuming devices and as a replacement for the large sized vacuum tube encouraged Lilienfeld et al. [9] in 1930 to give the basic concept for Field Effect Transistor (FET) but was unable to demonstrate its structure due to the presence of the surface states at the interface of oxide and semiconductor that prevents the electric field from penetrating the semiconductor material. However, this problem was overcome by Kahng and Attala [10] who invented the first ever insulated gate FET by using the combination of three layers i.e. metal (M), oxide (O) and semiconductor (S). Moreover, the presence of the grown silicon dioxide layer on semiconductor surface reduces the amount of surface states initially present and gave the name MOSFET (Metal Oxide Semiconductor Field Effect Transistor).

Table 1 Milestones in the bulk technology [11].

Year	Technology	Channel Length (um)
1960	MOSFET	-
1969	Ion-implanted channel	-
1971	Intel 4064 Microprocessor	10
1979	Silicided polysilicon gate	1
1986	Retrograde channel doping	0.5
1993	Copper interconnect	-

Several milestones in bulk technology as very effectively summed up by Wong et al [11] as shown in Table 1 starting from the invention of MOSFET in 1960, the production of ion-implanted channels, with further the invention of the first Intel

4064 microprocessor. The author [11] has also pointed out other advancements such as the silicided polysilicon gate to retrograde channel doping and the use of the copper interconnect which further increase the performance parameters, i.e. increases drain current, reduces the leakage current, of the MOSFET.

Since then, a MOSFET is used as a fundamental switching device with four terminals as shown in Fig.1.2 (Gate, Drain, Source and Body) in very large scale integrated (VLSI) circuit that is controlled by the electric field applied to one of the terminal that is a gate.

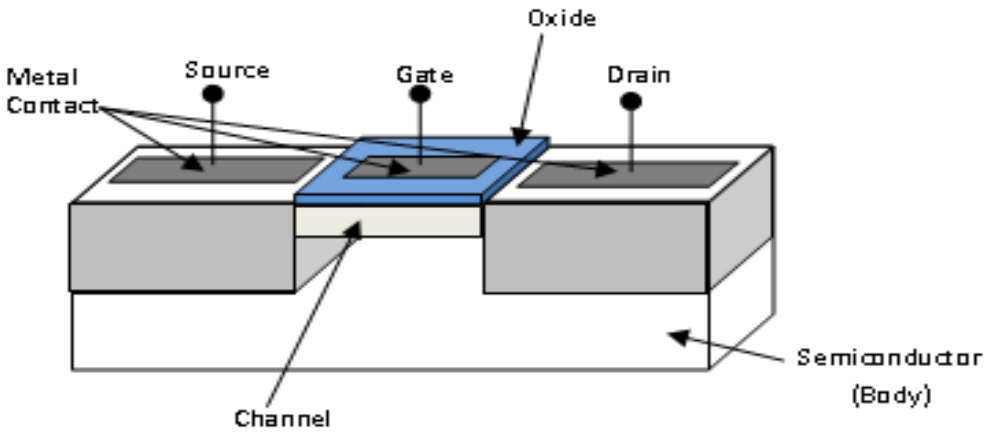


Fig.1.2 The four terminals MOSFET Structure.

Moreover, the terminals drain, source and gate are highly doped, but the body is lightly doped. The gate electrode is made of metal or poly-silicon and is separated from silicon body with a thin insulating film which acts as an energy barrier between the gate electrode and silicon body. The conductive region of the device may either be p-type or n-type depending upon the application. However, with proper bias condition a significant current can flow between the source and drain terminals of the MOSFET which makes the possibility of two types of current flow in the device: 1) Diffusion current which is the dominant current when applied gate voltage is less than the threshold voltage and 2) Drift current which is dominant when the applied gate voltage is greater than that of the threshold voltage. On the basis of the flow of current between the drain and source, three operating regions are feasible [12-14]:

1) Cutoff region, where no current flows excluding sub-threshold current which become dominant when the dimensions of the device becomes significantly smaller,

2) Linear region, where the linear current flows between source and the drain terminals, and

3) Saturation region, where the current gets saturated as the channel formed between the source and drain is pinched off at the drain side.

1.2. Scaling

To improve the system reliability, current drive, computational capability and integration density at lower cost, scaling should be applied [15]. The basic idea behind scaling [16, 17], lies in to produce smaller transistor with performance similar to that of the larger one and simultaneous reduction of all the dimensions. However, the geometrical ratio, (the ratio between the horizontal dimensions (channel width) to that of the vertical dimension (channel length)) should be maintained with precision.

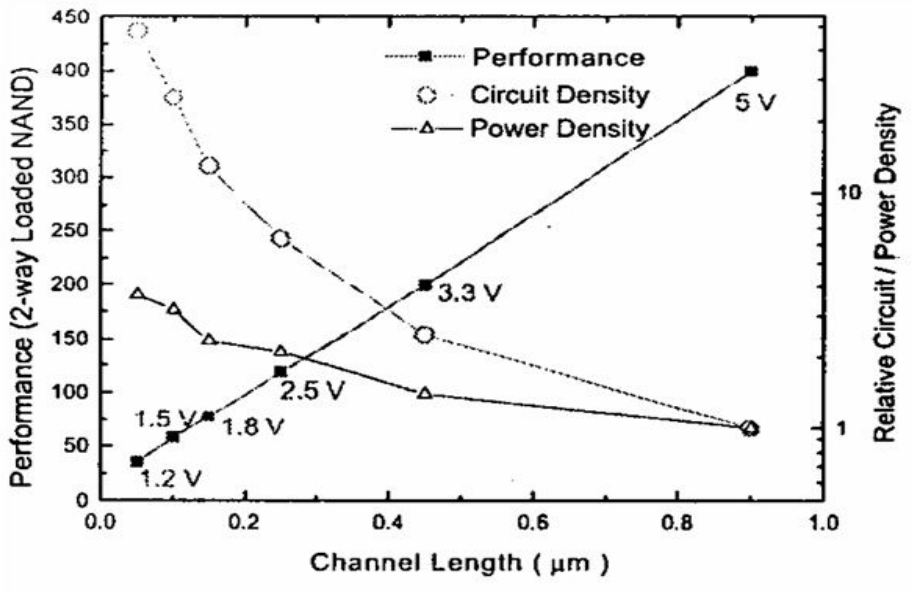
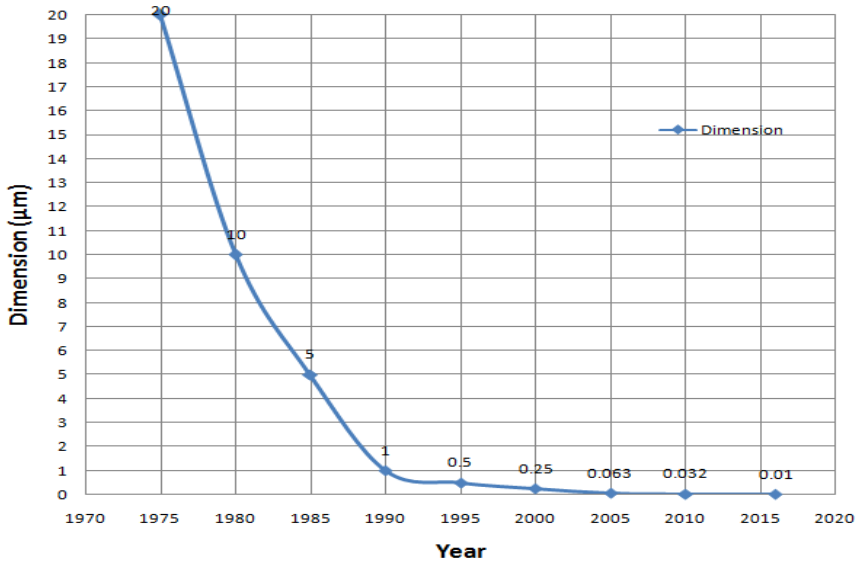
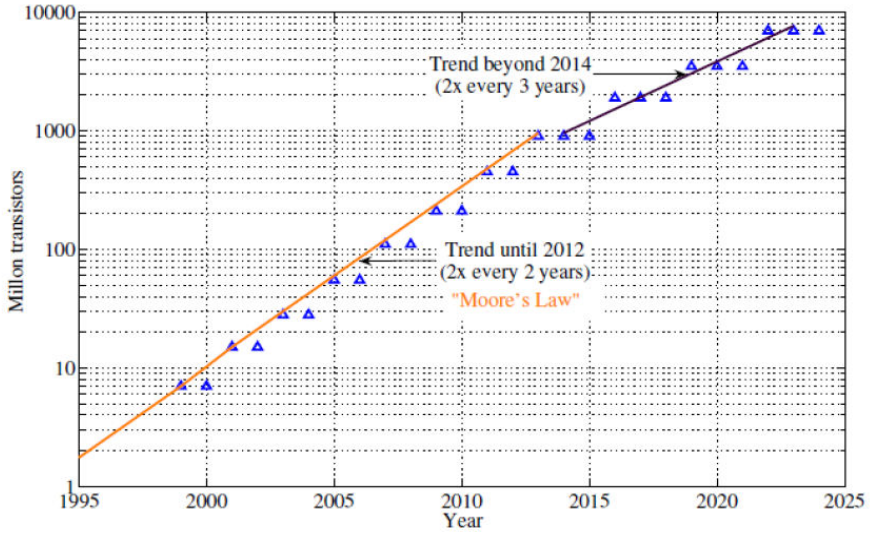


Fig. 1.3 Trends for CMOS performance, power density and circuit density [18].

Moreover, with the use of scaling, the reduction in the delay and further the advancement in clock frequency are seen. In addition to this, device density is doubled and reduction in energy and the active power per transition is also reported [18]. However, Fig. 1.3 also shows the linear circuit performance due to the technology scaling.



(a)



(b)

Fig. 1.4 (a) Technology progress [22] (b) Semiconductor Technology Road Map [Image source: ITRS update 2010].

Therefore, the semiconductor industry was encouraged to project the scaling theory in addition to the observation made by Gorden Moore [19, 20], in the form of International technology Roadmap of Semiconductor (ITRS) [21]. Fig. 1.4 (a) forecasts the dimension reduction over the year through the ITRS roadmap, and Fig. 1.4 (b) suggests till 2014 the doubling of transistors will follow Moore's law, after that the pace of advancement (i.e. doubling) will slow down to every 3 years. Fig. 1.5 suggests the conceptual idea for scaling, were a, W, W_d, L_g and t_{ox}, represents the scaling factor, wiring width, depletion depth, gate length and oxide thickness respectively.

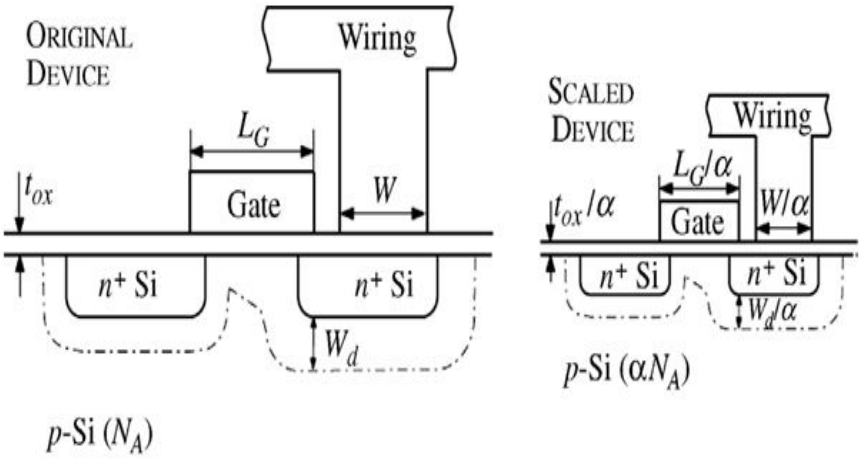


Fig. 1.5 The schematic diagram of device scaling [16].

However, based on the idea the classical scaling techniques can be classified into two types: [14]

1) Constant voltage scaling and
2) Constant field scaling.

In the constant voltage scaling [23], all the dimensions of device are scaled-down keeping the power supply voltage and terminal voltages unchanged so as to remain compatible to prevailing electronic system regarding supply voltage standards. However, this scaling technique is not a practical one, as the power dissipation increases to a high level which leads to the electro-migration, hot carrier degradation and oxide breakdown [24]. Moreover, in the constant field

scaling introduced by Dennard et al. [16], all the voltages and the dimensions are scaled down, while doping as well as current densities are increased by the scale factor α, keeping the vertical field constant. In addition to this, the speed of circuit is also enhanced by the same factor α and circuit density increases by α^2, however, the problem arises when the horizontal field keeps on increasing as the dimension of device become significantly smaller, creating problems on the potential barrier at the source end [25]. Also, the voltages, sub-threshold slope and off-current are not scaled well as the length scale down, which violates the constant field scaling technique [26]. Therefore, Baccarani et al. [27] has proposed more generalized scaling technique in which the vertical and horizontal fields are changed by the same multiplication factor. Although, the shape of electric field is preserved now, it has potential issue such as significant enhancement in the power density. Brews [28, 29] also proposed a scaling method called sub-threshold scaling which does not stress on specific factor for scaling individual dimensions and allows independent manipulation of a large number of variables as long as the remaining variables compensate for these changes. The summary of these scaling is shown in Table 2.

However, the above mentioned scaling techniques only tell about how to shrink the device, it does not tell anything about the limit of the scaling. There are certain physical phenomenon's which limit these scaling techniques such as quantum mechanical tunneling, that happens as the barrier existing in MOSFET becomes very thin and the random dopant fluctuation, due to the present manufacturing techniques.

In addition to this, the power supply scaling also has a limit which is the thermal voltage [30]. The Si band-gap potential (E_g/e) is also the major parameter which cannot be scaled down, and as the supply voltage is scaled down the effect of band-gap potential increases which results in increase in electric field and the depletion depth. Here, the band gap potential can only be changed by changing the semiconductor itself. As the electric field increases, it confines more charge carrier closer to the surface, which further reduces the mobility, increases the

quantum confinement energy and the gate depletion, consequently the threshold voltage is increased.

Table 2 Scaling techniques [16].

Physical parameter	**Constant Electric Field Scaling Factor**	**Generalized Scaling Factor**	**Generalized Selective Scaling Factor**
Channel length, Insulator thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Channel width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric Field	1	ϵ	ϵ
Voltage	$1/\alpha$	ϵ/α	ϵ/α_d
On-current	$1/\alpha$	ϵ/α	ϵ/α_w
Doping	A	$\epsilon\alpha$	$\epsilon\alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w{}^2$
Capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Power dissipation	$1/\alpha^2$	ϵ^2/α^2	$\epsilon^2/\alpha_w\alpha_d$

Moreover, several methods are utilized to reduce the threshold voltage, i.e. retrograde doping profile and the body biasing relative to source etc [31, 32]. Therefore, there is a need of proper selection of power supply voltage and threshold voltage [33].

While it is widely believed that CMOS will still be the dominant technology in the near future, practical and fundamental limits of CMOS scaling poses tremendous challenges beyond the 45nm technology node. In addition to this the major challenge faced by the circuit designers is the Short channel effects (SCE).

1.3. Short Channel Effects

When the MOSFET channel length that is the distance between source and drain in the MOSFET, is comparable to the depletion depth of the source and drain under a gate with zero drain-source voltage, the device is considered to be short. As the dimension of device shrinks significantly more, the short channel effects (SCE) dominates over the device performance [34] and attributes following two physical phenomena:

1) The restriction imposed on electron drift characteristics in the channel, and

2) Alteration of the threshold voltage due to short channel length.

The Table 3 summarizes the various short channel effects.

Table 3 The SCE [34].

S.No	Effect	Reason	Reference
1.	Drain induced barrier lowering (DIBL)	As the drain voltage increases, the potential barrier of the channel decreases and allows the flow of electrons between the source and drain even if the gate voltage is lower than that of the threshold voltage.	[35-37]
2.	Surface scattering	The electric field component in the direction of current flow increases due to the extension of the depletion layer in the channel which further makes the surface mobility field dependent as the channel length becomes significantly smaller.	[38-39]

3.	Velocity saturation	For a short channel device, the current saturates because of the carrier velocity saturation in place of pinch-off point in bulk MOSFET and current is independent of gate-to-source voltage which happens when the dimensions of device are scaled down without lowering the voltages, therefore the trans-conductance reduces in the saturation-mode of operation.	[40-41]
4.	Hot electron effect	As the high energy electrons enter the oxide they are trapped, which giving rise to oxide charging that accumulate with time and degrade the device performance by increasing threshold voltage and affect adversely the gate's control on the drain current.	[42-43]
5.	Threshold voltage roll-off	As the field pattern generated by the gate is 2-D for short channel devices because of closeness of source and drain, the threshold voltage varies with the channel length. The part of the channel is already depleted, therefore significantly less voltage is required for the operation of MOSFET as the threshold voltage decreases.	[27]
6.	Punch-	Due to the proximity of drain and	[44]

	through	source, the depletion region of the drain and source extend into the channel and merge. Therefore, the current flow between the source and drain which cannot be controlled by the applied gate bias.	
7.	Oxide tunneling current	As the oxide thickness reduces the electric field increases, which further forces the current to flow in the gate terminal.	[45-46]
8.	Reverse short channel effect	The retrograde doping profile results in point defects at the surface edge where the impurity atoms pile up and increases the channel doping closer to the source/drain region. For the short channel devices the region with the enhanced doping is a significant part of the channel. Therefore, the increase in doping in addition to the reduced channel length causes the threshold voltage to increase with scaling until eventually short channel effects take over.	[47]
9.	Gate induced drain leakage (GIDL)	The electric field due to the drain can cause the overlap region to form a depletion region and if this field is significantly high it may invert the surface to p-type. When the channel is being formed the carriers are swept in	[48-49]

		this p-well. The effect of the increase in the oxide thickness is more significant to GIDL as compared to that of the gate length.	
10.	Mobility degradation	For the short channel devices, one reason for the decrease in mobility is the velocity saturation, which occurs due to the presence of electric field perpendicular to the gate. The electrons slow down by the increase in scattering, thereby decreasing the mobility with respect to the bulk MOSFET. Also, as the surface is rough, more scattering is there.	[50-51]

However, the reduction of SCE is of prime concern while maintaining the better device performance in nano-scale regime. Therefore, several methods have come up with some negative effects such as performance degradation and additional leakage. The increase in channel doping so that the electric field lines that originate from the drain and propagate to the source are terminated, however, this high level of doping degrades the low field mobility of the carrier as the impurity scattering is increased, which further reduces the drive current [52]**.** Moreover**,** it also increases the gate-induced drain leakage (GIDL) and band-to-band tunneling across the reverse-biased drain junction. In addition to this, the significantly more threshold voltage variation is observed due to the statistical fluctuation of channel dopants, mainly in the nano-scale regime [53]**.** The reduction of oxide thickness is important for improving the gate control on the channel, however, this causes tunnelling and results the leakage current when the thickness of the oxide reaches 2 nm and further increases standby power [54, 55, and 31]**.** However, with the lowering of source/drain junction depth to reduce drain coupling to the source

barrier, the doping density has to be increased, however this doping density has an upper limit for solid solubility. Therefore, the series resistance increases and degrade the device performance [56]**.** Table 4 suggests the certain scaling limits which introduce additional problems of short channel effects (SCE).

Table 4 Limits of scaling [57].

Feature	**Limit**	**Reason**
Oxide thickness	2.3 nm	Leakage(I_{off})
Junction Depth	30 nm	Resistance(R_{sd})
Channel Doping	V_{th}= 0.25V	Leakage(I_{off})
Channel Length	0.06 µm	Leakage(I_{off})

Moreover, by the scaling the dimension the MOSFET the processing speed can be enhanced and further improve RF performance. The important metrics for RF MOSFET circuits are the maximum oscillation frequency and cut-off frequency. The former is defined as the frequency at which the current gain of the device becomes unity and later defines the frequency at which power gain becomes unity. However, both these metrics relate to the trans-conductance and parasitic capacitance. As the dimension of the device reduces, the cutoff frequency of the device increases to up to 400 GHz. Noise figure is also one of the other important figure-of-merit. However, Song et al [58] have purposed a new figure-of-merit for low noise amplifier and also predicted the close optimum gate voltage to maximize this figure of merit.

Therefore, Fig. 1.6 shows the advances in MOSFET technologies which have continued, with further increase in the cutoff frequency (f_T) of the devices [59]. Moreover, due to relatively high f_T values, the bulk-silicon MOSFET device is becoming a viable technology choice in the analog and RF applications for portable wireless communication systems.

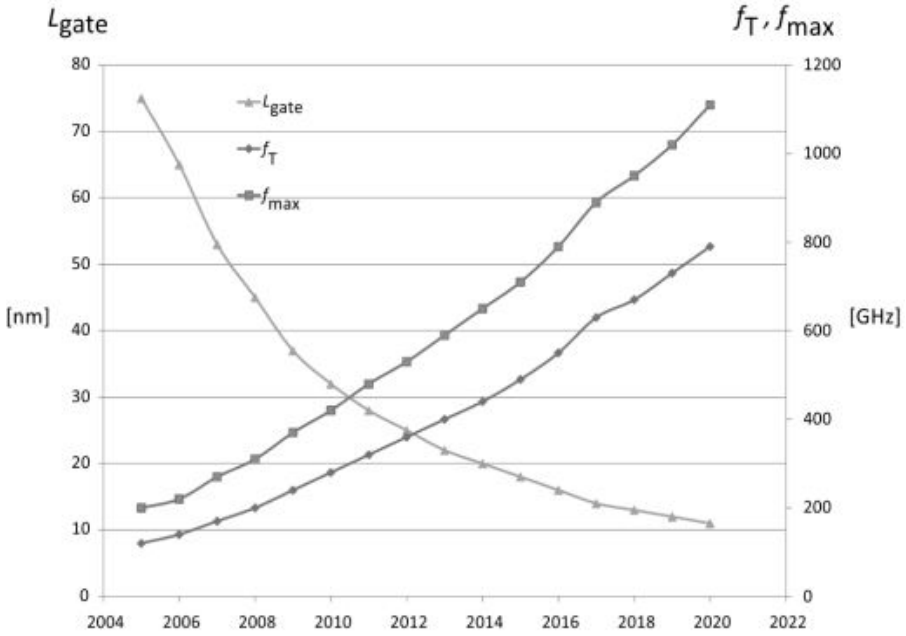


Fig. 1.6 Trend of MOSFET scaling [59].

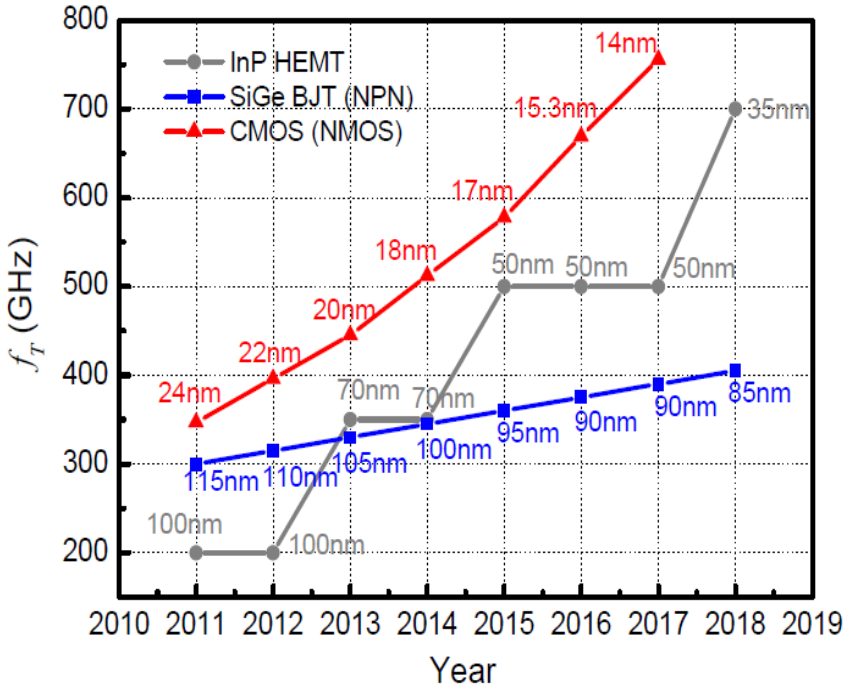


Fig. 1.7 The current-gain frequency variation over the years [ITRS 2011 update].

However, it can also be seen through Fig. 1.7 that a high value of the current gain frequency can be achieved with the CMOS technology. However, with 18 nm

technology, the f_T is achieved to be is 511 GHz, which shows that the CMOS has an advantage for high speed applications in future communication system.

In addition to this, the low power dissipation of the device is required for the applications such as battery operated single-chip typical wireless transceiver [60], which can be achieved by reducing the device supply voltage. Therefore, the communication market has reached a revolutionary era with the various forms of improvement in the MOSFET structure. Moreover, the circuits formally implemented as a discrete structure, now, which is implemented on the single chip. Therefore, the system on chip is no longer a mere idea. Due to the high unity gain of MOSFET, it becomes an attraction for the RFIC circuit designers [61]. However, it is observed that, the MOSFET must be operated in the moderately inverted region to achieve the desired circuit performance in ultra low power RFIC design [62]. In addition to this, Lee and Cheng [63] have analyzed the MOSFETs, which has higher low-frequency limit (LFLs) as compared with BJTs which is useful for RFIC design as well as generating HF distortion model for MOSFETs and recently new technologies acting as a driving force in the personal wireless communication market.

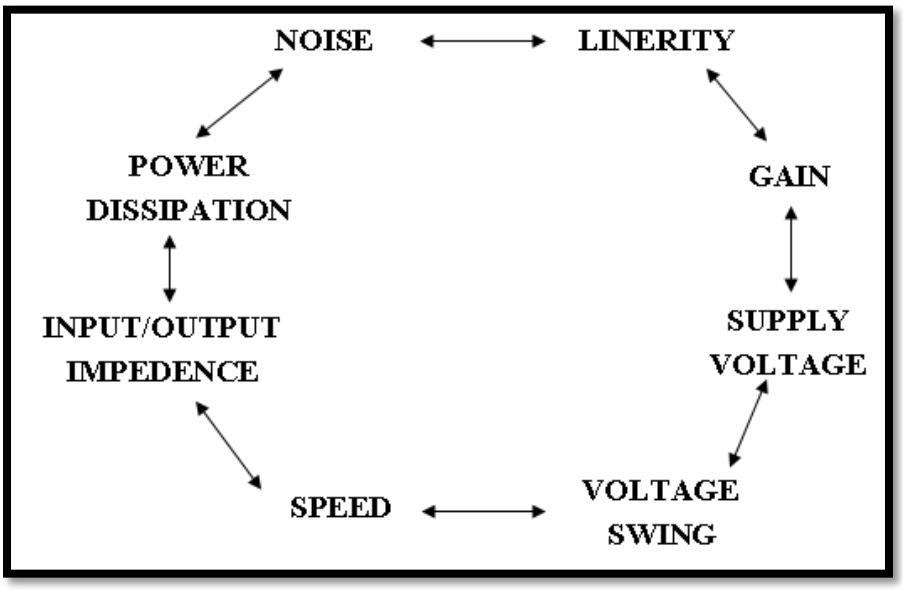


Fig. 1.8 The analog octagon [64].

However, Razavi [64] has shown the difficulty in using the digital MOS technology for the analog application, that is only one trade-off is optimized, i.e. power-speed trade-off, although a multidimensional design space in the form of the octagon as shown in Fig. 1.8 is presented where every parameter trade-off with each other. For example, to lower the noise of a front-end amplifier, we must consume a greater power or sacrifice linearity or to increase the gain of the amplifier, we have to work on high supply voltage or sacrifice linearity. In addition to this, if the supply voltage is reduced, power dissipation may increase. Woerlee et al [65] have confirmed the higher potential of CMOS for RF applications at GHz frequency.

Table 5 The recent single chip transceivers for different applications.

S. No	Technology	Application	Reference
1.	0.090 µm	5 Mbps transceiver with energy harvesting module for wireless sensor network	[66]
2.	0.18 µm	2.4 GHz low rate wireless personal area network (WPAN)	[67]
3.	0.090 µm	2.4 GHz low power Zigbee transceiver	[68]
4.	0.028 µm	Phase modulated continuous wave radar at 79 GHz	[69]
5.	0.13 µm	24 GHz UWB transceiver with self organizing localization network	[70]
6.	0.13 µm	3-10 GHz front-end transceiver used for low power biomedical radar	[71]

Recently, many transceiver chips using the CMOS technology has been developed, as summarized in Table 5. Moreover, the reduction of feature size of the device based on the channel, and gate engineering [35] also introduces additional parasitic and new phenomenon such as SCE, parasitic source/drain resistance, poly-silicon depletion layer effect, ballistic transport, carrier energy quantization, bias dependent parasitic capacitances etc. As the fabrication processes also limits the scaling, novel techniques have to be introduced to keep the pace with the scaling to yield the desired throughput, and to retain the progress in device scaling technology.

To move forward in the direction to achieve better performance, novel material and device structures, which are the non-conventional structures, are required beyond 65nm technology **[**72**].** Moreover, Rue et al [73] analyzed that the output power capability of the transmitter will degrade as the device will scale down due to the hot-carrier injection and reducing the oxide will not be effective. Therefore, the innovated device structures can reduce the short channel effects (SCE), therefore they would be a better choice to be used in the future transceiver chips, which are discussed in the following section.

1.4. Advanced MOSFET Structures

In the silicon-on-insulator (SOI) technology, the presence of buried oxide layer below the transistor junction reduces the junction capacitances and reverse body effect, which provides a faster and less power consuming device, has been considered as one alternative to the conventional bulk MOSFET which offer performance as expected from the next generation Silicon technology [31]. Moreover, by using the buried oxide layer the fringing capacitances are suppressed, that provides better processing speed [74]. However, the fully-depleted MOSFET improves the short channel effect (SCE), transistor scalability and circuit performance [75, 76]**.** The introduction of ultra-thin SOI technology offers the significant advantage of reducing the leakage paths by stopping the penetration of the drain electric field in the source region. However, this device

suffers from degradation in the on-state current due to mobility degradation and increase the external resistance, which can be rectified by the use of the thin gate spacer with raised source/drain process. In addition to this, the threshold voltage control with the use of doping is difficult, therefore the poly-silicon gate is replaced with a metal silicide gate where it is controlled by the work function engineering by the gate. Moreover, the mobility degradation due to the surface roughness is still an issue when the body thickness reaches up to 5 nm [77]. For fully depleted SOI MOSFETs, the drain electric field penetrates though the buried oxide into the channel region, thereby resulting in a large impact on the channel electrostatics. However, the bulk MOSFETs and DG MOSFETs can achieve better short-channel effect compared to that of the fully depleted SOI MOSFETs due to the screening of the channel by the bottom layer. Therefore, with the advantages of high processing speed, lower power dissipation and consumption, high tolerance to radiations and low value of parasitic capacitances, some other unavoidable issues come into picture when the SOI dimension reaches to nanometre regime [75]**.**

To seek possible alternatives for bulk MOSFETs beyond the 45nm technology node, a number of novel multi-gate MOSFETs have been proposed, including Surrounding Gate, Pi-Gate [78], Omega-Gate [79], Tri-Gate [80] and Double-Gate (DG) MOSFETs. Various numerical simulations and analytical analysis have shown better scalability of multi-gate MOSFETs over the bulk MOSFETs. The improved scalability allows multi-gate MOSFETs to scale down to shorter gate length with the same off-current or produce less off-current with same gate length, thereby achieving better power-speed product. Among these new emerging devices, the DG MOSFET is most promising because of its compatibility with the conventional planar technology. In addition to this, DG MOSFET reduces the fringing field through drain-to-body which further improves the device scalability, and the mobility requirement in this structure is less as compared to the bulk MOSFET due to less vertical field. However, the mobility can be enhanced by using the following techniques: 1) strain engineering

and 2) orientation effects [81]. Therefore, more enhanced versions of SOI structures come into the picture, which is a thin body fully-depleted SOI MOSFET, raised source and drain fully-depleted SOI MOSFET, metal source and drain fully-depleted SOI MOSFET and multiple-gate fully-depleted SOI MOSFET. Recently, to advance the scaling of MOSFET technology the double-gate MOSFET and surrounding gate MOSFET using lightly doped and ultra-thin body layer is an emerging research area [82]. Moreover, for the advancement in the technology in the wireless communication field, the standard MOSFET structures using the standard CMOS technology should be replaced by more innovative structures such as double-gate MOSFET and surrounding-gate MOSFET. The advantages of these structures for the operation in the high frequency regime of spectrum are discussed in the following section.

1.4.1. Double Gate MOSFET

The main design objectives of DG MOSFET are: 1) to reduce SCE and 2) to maintain good electrical characteristics [83]**.** The planer DG MOSFET is an extension of the single gate MOSFET that consists of two gates designated as a front-gate and back-gate, within which the ultra thin silicon layer is sandwiched [84]. The additional gate significantly increases the electrostatic gate control over the channel and these gates are effective in shielding the drain electric field-lines from reaching the source to reduce the potential barrier as well as reducing the SCE. Due to un-doped/lightly doped body, the problem of random dopant fluctuation is also absent. Moreover, both the gates contribute to inversion carriers, which have high drive capability and two channels for the current flow are formed, when these two gates simultaneously control the charge. In addition to this, as the silicon film is very thin there exists a good coupling between the front and back gate, which affect the terminal characteristics of the MOSFET. Fig. 1.9 shows the schematic of DG MOSFET.

In the common mode operation, both the gates are switched simultaneously, however for other possible mode of operation, a back gate bias is applied to create

a conducting plane, and switch the front gate which provides an additional parameter for the circuit design. Therefore, two types of structures are possible:

- Symmetric DG MOSFET (SDG MOSFET): Both the gates have identical work function. However, the threshold voltage can be adjusted with the help of work function of gates. The thin silicon substrate is under volume inversion condition, therefore the conduction of carriers is across the entire volume of material as compared to that of the bulk devices.
- Asymmetric DG MOSFET (ADG MOSFET): Both the gates have different work function. However, the threshold voltage can be adjusted by changing the body thickness and gate oxide thickness without need for special gate material. In the asymmetric double gate device, two oxide thicknesses are unequal, the two gates have different flat-band voltage and two different gate biases. In the asymmetric DG MOSFET with a mid-gap gate electrode, the bands in silicon are not flat in the sub-threshold regime [85].

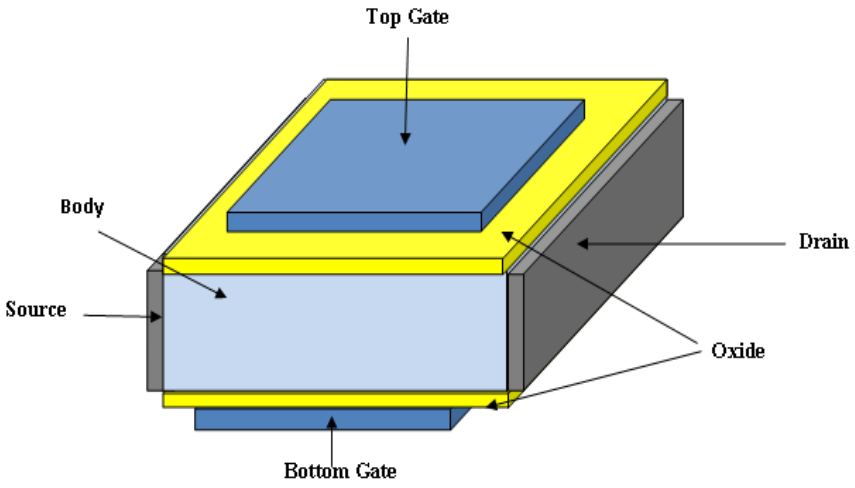


Fig. 1.9 The Schematic of the double gate MOSFET.

Moreover, there are two operating modes for DG MOSFETs [86]:

- Three-terminal mode: The three-terminal mode refers to the situation where the two gates of DG MOSFET are electrically connected and switched, simultaneously.

- Four-terminal driven (or independently driven) mode: When operated in four-terminal driven mode, the two gates are biased differently with only one gate switching. The four-terminal driven mode enables the possibility of dynamic threshold voltage adjustment in circuit design and thus enlarges circuit design space.

Fig. 1.10 shows the different structures and two operating modes of the DG MOSFET. However, the four-terminal driven DG MOSFETs exhibit non-ideal sub-threshold slope. This is because the potential across the silicon film does not move along as a whole with the switching gate if the potential of the non-switching gate is fixed. Moreover, the four-terminal driven DG MOSFET also shows worse short-channel effect than the commonly used three-terminal driven DG MOSFET.

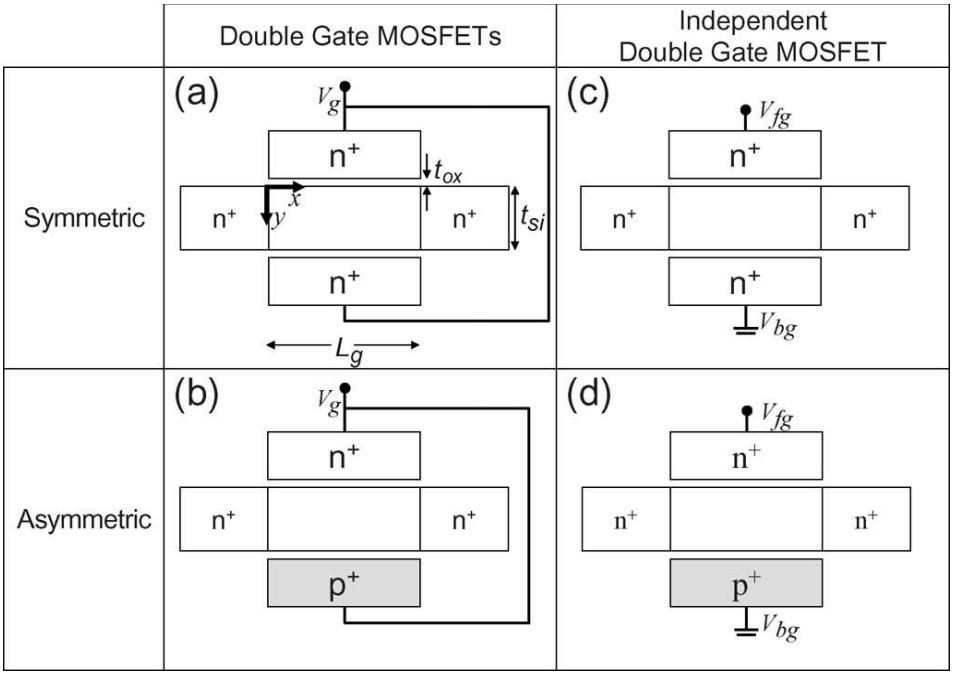


Fig. 1.10 The schematics of DG MOSFET structure. (a), (b) tied gates and (c), (d) separated gates. [86].

Due to high gate-to-substrate coupling, the device produces a near ideal sub-threshold slope (60 mV/dec) and flexible threshold voltage control can be offered by the separation of the two gates [87]**.** This device has less parasitic capacitances

as compared to that of the conventional MOSFET, however the important thing is the proper alignment of the front and back gate, as the misalignment contributes to the parasitic capacitances. The thickness of body has to be controlled to reduce the parasitic resistances, which are in the series with the channel and source/drain electrode. However, when the scattering due to impurity or coulomb scattering is absent, then the carrier mobility is significantly high. The carrier mobility degradation which is related to gate field reduces due to the lightly doped/un-doped substrate film for the given oxide thickness. However, as both the gates are close to channel, there is the dominant control over the channel electrostatics.

Moreover, double gate MOSFET has an advantage of the architectural feature which is useful for the design of extraordinarily radio frequency analog integrated circuits and adaptive systems, with less difficulty in fabrication processes. Although, it is pointed out that the device has much better potential in this form of application, if the top and bottom gates are driven independently [88], which further increases the operational capability, reduces the parasitic capacitances and layout area and increasing the speed with reduced the power consumption as compared to that of the conventional MOSFET's. Moreover, this is a useful method to tune the response of conventional CMOS analog circuits, especially, for current-mode design [89]. DG-MOSFETs cover the way for capable, tolerant and reduced circuit size with tuneable features.

1.4.1.1. Related Work

Various researchers/scientists have devoted their hard work in developing compact models for DG MOSFET. Balestra et al [90] demonstrated that the double gate MOSFET force the whole silicon body thickness in the strong inversion. The volume inversion effect is quite significant when the gate-source voltage is less than that of the threshold voltage. In addition to this, Taur et al [91] also presented an analytical model based on the charge sheet approximation for symmetric double gate (SDG) MOSFET and analyzed the threshold voltage (V_{th}), which is independent of the silicon body thickness (t_{si}). However, an exponential

decrease in the saturated value of current with the drain-source voltage (V_{ds}) is seen, as compared to that of the common piecewise models where the current is made to be constant in saturation.

Lu et al [92] have purposed the model based on the Poisson equation and the current continuity equation without the charge sheet approximation. Moreover, the authors presented the threshold voltage of ADG MOSFETs that is the function of silicon thickness. Therefore, the sub-threshold current is much more sensitive to the silicon film thickness, as compared to that of the SDG MOSFET. However, the ADG MOSFET with thicker silicon film has a lower threshold voltage and thus higher sub-threshold current.

Ortiz Conde et al [93] developed an accurate drain current model consistent with the drift-diffusion transport and based on the Pierret and Shields formulation which is valid for all the operating conditions. In addition to this, Ortiz Conde et al [94] also developed the analytical solution for the surface potential of un-doped body SDG MOSFET using the principle branch of the Lambert W function. However, for achieving the desired circuit performance of DG structure, Balasubramaniam et al [95] analyzed, the effective channel length, that is larger than the physical gate length and the circuit performance is enhanced by using the thin-body DG MOSFET. However, the effect of random dopant fluctuation and junction capacitances are reduced significantly as the lightly doped or undoped body is used. The variation in the source drain separation for achieving a better drive current can be performed, however trade-off between SCE with series resistance has to be maintained. The result illustrated that the optimal gate-to-Source-drain overlap for maximizing circuit performance is lesser than that needed to maximize the drive current [95]. Antoine et al [96] investigated the non-Colombian scattering, and the reason behind the degradation of mobility below 100 nm gate, ariseing because of the presence of neutral defects in Si or at the interface near the source and drain. The author also illustrated that the defects can be improved by annealing temperature from 1050 ^{o}C to 1080 ^{o}C. Mahapatra [97] investigated the effect of the gate and channel engineering on the leakage

current, drain induced barrier lowering (DIBL), which would further improve circuit speed and power consumption. The author's results demonstrate that the DG-DI MOSFET has better performance as compared to that of the other counterparts. The fringing induces barrier lower (FIBL) is studied by Charmi [98] which arises when the effective oxide thickness is comparable to the gate length. Moreover, the reduction of FIBL can be performed by using under-lap source/drain region. Evans et al [99] analyzed that the carrier penetration into the oxide is not accounted for in the density gradient method, therefore the first principle calculation can be used to optimize an accuracy of the density gradient method for modeling of the device. Moreover, the position of the impurity in the channel plays a significant role and it degrades the current in the device, therefore Dollufus et al [100] analyzed this effect on the single gate MOSFET as well as the DG MOSFET in addition to the velocity overshoot effect for both the device structures. The authors [100] illustrated that the degradation in the performance of single-gate MOSFET is more pronounced with more significant effect observed for the p-type impurity. For a DG MOSFET, the effect of negative gate overlap and the control of back gate bias is analyzed in [101], which illustrate that if the overlap is negative the device performance is degraded. However, if the back gate bias is high, the threshold voltage is reduced which further increases the circuit speed due to the increase in the ion and if the bias is low, the threshold voltage is increased, which can reduce the power dissipation. Therefore, depending upon the application a trade of can be maintained in high on-current and low power dissipation. Based on the charge coupling between the source and the drain end and the front and the back surface potential, Ortiz-Conde et al [102] developed the drain current and the trans-conductance model for the un-doped asymmetric double gate MOSFET. The variation of trans-conductance and the sub-threshold-slope is analyzed based on the variation of the back gate bias. Taur [103] has analyzed a un-doped body asymmetric DG MOSFET symmetry point shifts from the center to some point in the silicon body and is minimum at that point. Moreover, the threshold voltage dependencies on the dimensions of asymmetric DG MOSFET have been studied for the long- and short-channel and then

compared with the threshold variation with a symmetric DG MOSFET in [104]. Cakici and Roy [105] performed a case study on Schmitt trigger to analyze the effect of using connected gates or independent gates DG MOSFET and the results illustrates that high noise immunity at low dynamic power dissipation can be achieved by the independent operating gates. Although, an increase in the delay, leakage power and process variation are the significant undesirable by-products for the device performance. Moreover, the dynamic threshold voltage control is feasible with the use of independent gates DG technology. In addition to this, Ruchika et al [106] also explored the design possibilities of the double gate MOSFET for achieving low power application. Roy et al [107] developed a model for a low density of state material in Double gate MOSFET by using both Fermi-Dirac statistics and field dependent diffusivity. A compact model has been developed in [108] for a junctionless double gate MOSFET. Mattausch et al [109] pointed out that to the future requirements of the technology, the surface potential model based on drift- diffusion approximation is essential.

However, Wie et al [110] have showed that, the minimum channel length of the DG SOI MOSFET can be reduced to 30% as compared to that of the conventional MOSFET, which would further increase the cutoff frequency and making it a better candidate for low voltage and low power applications. Kumar et al [111] explored the influence of channel and gate engineering on the analog/RF performance of DG MOSFET and analyzed that the gate and channel engineering, which increases the gain by 45%, 35% respectively compared to that of the single gate MOSFET. However, the channel engineered devices shows the reduction of the cutoff frequency. The advantages of triple material DG MOSFET over the dual material and single material DG MOSFET are discussed in [112]. The authors have analyzed the performance enhancement in terms of the intrinsic gain of 20.41% and 38.53% for dual material DG MOSFET and the triple material DG MOSFET respectively, unity gain frequency of 14.23% and 26.4% for dual material DG MOSFET and the triple material DG MOSFET respectively, and maximum oscillation frequency of 13.9%,23.85% for dual material DG MOSFET

and the triple material DG MOSFET respectively, which shows the device structure can provide enhanced performance for high frequency RF applications. Kumar et al [113] analyzed the SCE reduction and RF performance enhancement of the single halo dual material DG MOSFET compared to the single halo counterpart. The realization of high performance analog and RF circuits is possible by the use of high dielectric gate stack DG MOSFET [114].

1.4.2. Surrounding Gate MOSFET

The structure of the surrounding gate MOSFET is similar to the double gate MOSFET only the difference lie in that the channel is surrounded by the gate from all sides which reduces the leakage current in the device and further the performance of the device increases. Moreover, it also provides, approximately 30% reduction in the length of the device is achieved than that of the double gate MOSFET with a given silicon body thickness (t_{si}) and oxide thickness (t_{ox}) [115] which further increases the packing density. The flow of current is vertical along the cylindrical Si/SiO2 interface and the gate length of the transistor is defined by the height of the gate material. The tight capacitive coupling in all direction reduces the SCE. The General Surrounding gate MOSFET structure is shown in Fig. 1.11. However, the vertical orientation of the device on a single chip reduces the chip area and is also a much researched area.

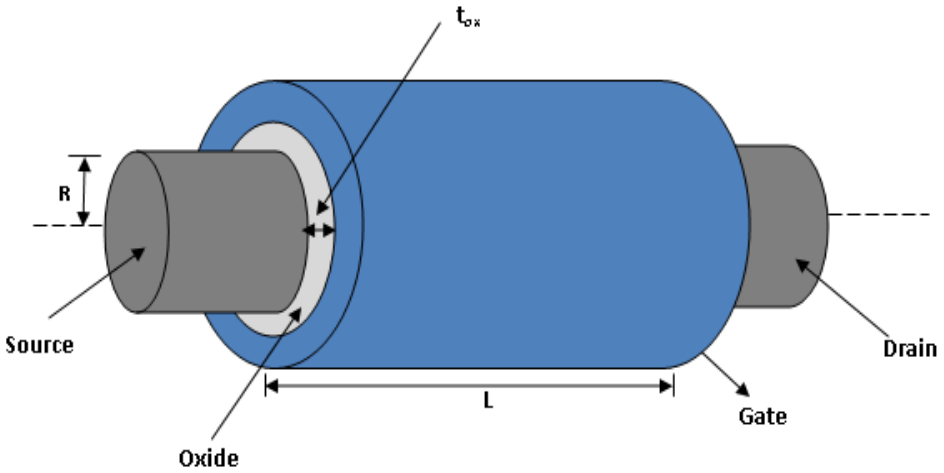


Fig. 1.11 The Schematic of surrounding gate MOSFET.

1.4.2.1. Related Work

The surrounding gate MOSFET is very effectively scaled down to the nanometer regime for low power and high speed applications [116]. Rustagi et al [117] have analyzed the surrounding gate MOSFET, is very effective for the high speed and low power circuit application. Iniguez et al [118] developed a DC model for surrounding gate MOSFET based on the charge controlled model, and the continuity of the channel current, which is preserved throughout all the operating regions therefore the model is effective for circuit simulations. Jimenez et al [119] also developed a model for the lightly doped surrounding gate MOSFET without any fitting parameter. Bian et al [120] have derived a model based on both the drift and diffusion current components based on the analytical potential approach, including the potentials at the oxide silicon interface and silicon center. Yu [121] has developed a model for the depletion mode surrounding gate nano-wire FET with capturing the conduction mechanism from sub-threshold to saturation region. The model for surrounding gate MOSFET is developed by taking into account the polysilicon depletion effect [122]. However, Roy et al [123] have developed a model for the surrounding gate MOSFET based on the Gaussian law instead of the Poisson equation. A potential based model for the dual material surrounding gate MOSFET before the onset of strong inversion, is analyzed in [125] based on the parabolic approximation to understand the short channel effects due to gate engineering. A new technique of general series solution method [126] is also developed for solving the cylindrical Poisson equation which is very effective in observing the various short channel effects that is threshold voltage, drain induced barrier lowering (DIBL) etc. The high level of doping and ultra thin oxide is a major requirement to reduce these short channel effects. Pandian and Balamurugun [127] have proposed a threshold voltage based model for the short channel surrounding gate nano-wire transistors with two forms of geometry that is junction based surrounding gate MOSFET and rectangular surrounding gate MOSFET. The major difference between these two geometries is the rectangular gate device is bound to get affected by corner effects much more in comparison

with the cylindrical gate device. The model for surrounding gate MOSFET including different fringing gate capacitance is developed [128], which is valid for the short channel devices with L_g= 15 nm and long channel devices with L_g= 50 nm. However, based on the charge control model, the authors in [129] developed an analytical expression of the total capacitance of un-doped body surrounding gate MOSFET as the function of voltages. Kranti et al [130] have developed a model for the short channel surrounding gate MOSFET accounting for the effect of field dependent mobility, velocity saturation, and source-drain resistance effect.

Ruiz et al [131] have developed a model for the total gate capacitance of surrounding gate transistors and based on the result the authors have compared the capacitance behaviour of the DG MOSFET and surrounding gate MOSFET and illustrated that the capacitance is less in surrounding gate MOSFET as compared to DG MOSFET due to the greater confinement by the gate.

A comparative study of the single material gate and gate material engineering surrounding gate MOSFET is performed in [132]. In addition to this, the effect of interface trap charges on the RF and linear distortion analysis is also presented. The results indicate that the gate material engineered surrounding gate MOSFET provides a better immunity against the interface charges and can maintain efficient device linearization, which makes the device useful for the radio frequency integrated circuit application. Sarkar et al [133] have analyzed the performance potential of the SRG MOSFET in the RF/Analog circuit's applications and discusses the performance of the device without including the quantum mechanical effects. Moreover, for the analog performance, high value of the trans-conductance generation factor (g_m/I_d) is needed.

With the development of the surrounding-gate MOSFET in the nano-meter regime, the high frequency capability of the transistors has reached to the GHz regime which is well suited for the radio frequency circuit applications [134, 135]. Hagh and Bindal [136] have discussed due to the full gate control over the channel, the vertical surrounding gate MOSFET can achieve low off-state current,

which makes the surrounding gate MOSFET as a promising device for very large scale integration technology. Moreover, the gate material engineered transistor shows better immunity against the influence of interface trap charges and exhibits significant enhancement to maintain the device linearization, as compared to a single material gate junction-less surrounding-gate MOSFET, so that it can be used as a high-efficiency linear radio-frequency integrated-circuit design and wireless applications [137]. Gautam et al [138] have analyzed the gate all around MOSFET with the vacuum as the dielectric, which is a better candidate for the high speed RF applications. Although, the trans-conductance and on-state drain current is reduced, but it can be enhanced by using the gate and channel engineering. Moreover, the double material gate gradual channel gate all around MOSFET has the highest cutoff frequency. However, the dual material gate junction-less nano-wire transistor [139] has an advantage of high on-state drain current high unity gain frequency and high maximum oscillation frequency, further which prove to be an efficient structure of the RFIC applications.

1.5. Problem Statement

The demand of the communication industry is increasing for the developments of the devices to handle high data rate and further the high frequencies. Moreover, the improvement in the communication market is also critically dependent on the dimension reduction of the devices. However, the conventional scaling, a tool for the MOS technology advancement into the nano-scale regime, has been hindered by many factors like the short effects (SCE), channel carrier mobility degradation, the hardiness of the circuit with respect to the process variations, etc., that is a vital concern for the circuit designers, which further results in the significant control of the drain on the channel potential. Therefore, the potential need is to minimize the effects of the drain on the channel potential that inspire numerous researchers/scientists for other non-conventional structures like SOI, pie-gate, and omega-gate MOSFET. However, recently, a lot of importance is being given on the double-gate (DG) MOSFET and surrounding gate MOSFET, as these devices scale down to the shortest channel length possible for a chosen oxide thickness,

which further reduces the short channel effects. Therefore, this study focuses on the Double-gate MOSFET and surrounding-gate MOSFET modelling and device characterization.

1.6. Dissertation Organization

This chapter describes the field of study and reviewed previous relevant literature. However, the key research issues and challenges are also identified. The remainder of the chapters is discussed as follows.

Chapter 2 discusses the symmetric DG MOSFET with its design philosophy and working operation. Further, the performance of the symmetric DG MOSFET based on the potential distribution, sheet charge, drain current, terminal charges and trans-capacitance are also analyzed based on the purposed simulation model.

Chapter 3 deals with the analysis of the surrounding gate MOSFET using the surface potential distribution, drain current, trans-conductance, output-resistance, on-state resistance, terminal charges, and trans-capacitance of the device. Moreover, the discussion on the effects of Gaussian doping on MOSFET performances such as the potential as well as the characteristics of the MOSFET is also included.

Chapter 4 discusses the basic performance parametric analysis of the double gate MOSFET and surrounding-gate MOSFET as a amplifier and as a switch through the use of the equivalent circuit approach which is useful for the analysis of the dynamic performance of certain MOSFET.

Finally, in **Chapter 5**, we summarize our work and suggest various directions in which this research can be extended in the future.

CHAPTER 2
PERFORMANCE ANALYSIS OF DOUBLE-GATE MOSFET

2.1. Introduction

Balestra et al. [90] purposed the first double gate MOSFET with significant volume inversion effect. Currently, the double-gate MOSFET is a subject of intense VLSI research and seen as a replacement for conventional bulk MOSFET beyond the 45 nm technology [140] as it can be scaled to the shortest possible channel length for a given oxide thickness and more electro-statically robust than the earlier reported MOSFETs due to the dual gate shielding and the reduced short-channel effects [77]. Fossum et al [141] have analyzed the higher processing speed of DG MOSFET as compared to that of the SG MOSFET. Fig. 2.1 shows the schematic of a Double Gate MOSFET and the Fig. 2.2 Illustrates the two major DG MOSFET structures: a) asymmetric type with both gates of identical work-functions ($\emptyset$) where both the surfaces channels turn on at the same gate voltage [142] and b) an asymmetric type with either different work function of the gates ($\emptyset, \emptyset'$) or different gate oxide thicknesses and only one channel turns on at the threshold voltage [84].

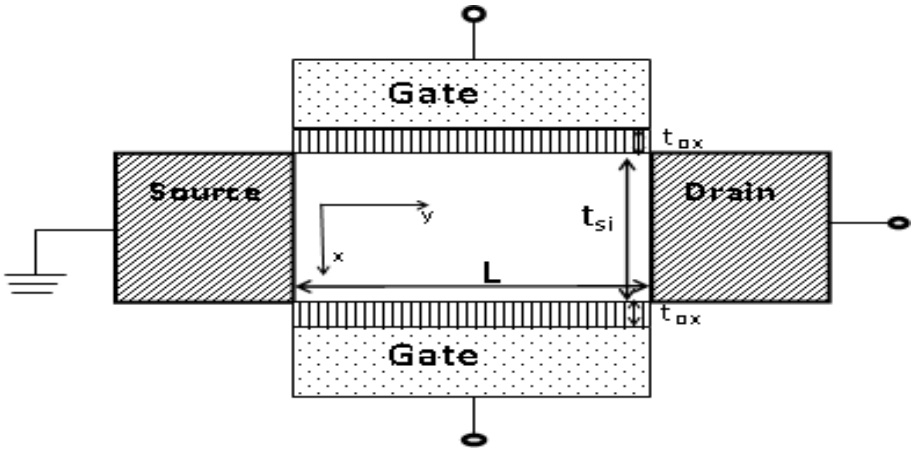
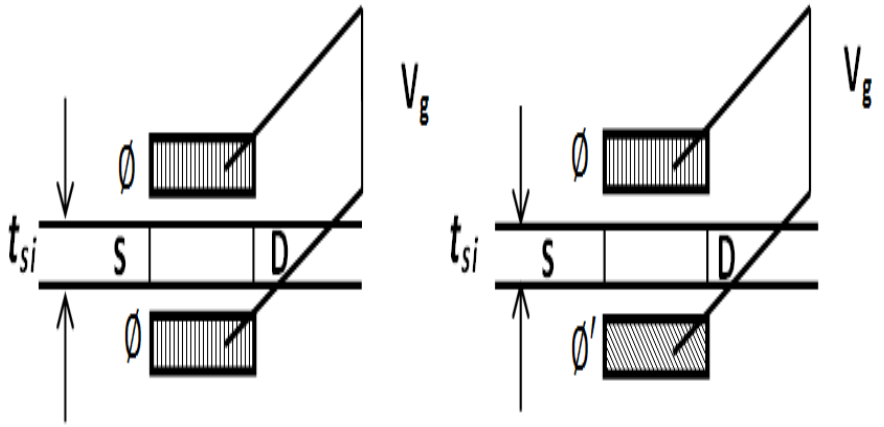


Fig. 2.1. Schematic of the DG MOSFET.



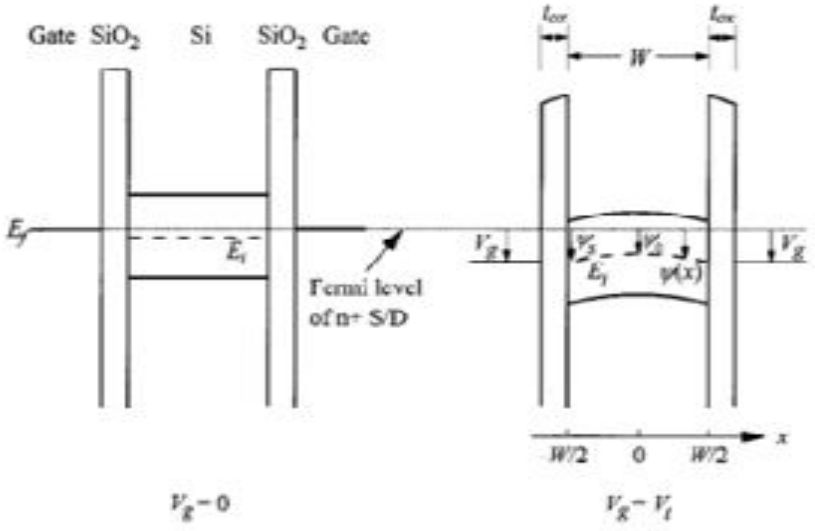
(a) (b)

Fig. 2.2 (a) Symmetric Double Gate MOSFET, (b) asymmetric Double Gate MOSFET.

Taur et al [143] derived the analytical model based on the charge sheet approximation which is applicable to all operating regions such as cutoff, linear and saturation. Yu et al [144] purposed an algorithm and the PSP model for the approximation of the surface potential of both the DG MOSFET and SG MOSFET. The model can cover all the operating regions without any use of fitting parameters or charge sheet approximation. The state-of-the-art of the compact models for un-doped DG MOSFET using the 1-D Poisson equation with the introduction of the SCE is discussed in detail in [145]. Riza and Roy [105], have studied the effect of using connected gates or independent gates DG MOSFET, and illustrated that the significantly higher noise immunity at low dynamic power dissipation can be achieved by the independently operating gates as it increases the gate-to-gate coupling. Singh and Jiang [146] showed that with the help of asymmetric DG MOSFET high performance and low power circuits are feasible in the nanometre regime. Therefore, this structure can be used in phase-locked loop where the requirement is a high speed, low voltage and low power operation [147]. Further, the other application of the symmetric DG MOSFET is as a fast switching device [148]. Recently, Srivastava et al. [149, 150] has analyzed the double gate MOSFET and cylindrical surrounding double gate MOSFET for the application as a double pole four throw switch.

2.2. Symmetric Double Gate MOSFET

The planer DG MOSFET is an extension of the single gate MOSFET that consists of two gates designated as front-gate and back-gate, within which the ultra thin silicon layer is sandwiched [83]. The additional gate significantly increases the electrostatic gate control over the channel and these gates are effective in shielding the drain electric field-lines from reaching the source to reduce the potential barrier as well as reducing the SCE. Due to un-doped/lightly doped body, the problem of random dopant fluctuation is also absent. Moreover, both the gates contribute to inversion carriers, which have high drive capability and two channels for the current flow are formed, when these two gates simultaneously control the charge. In addition to this, as the silicon film is very thin there exists a better coupling between front- and back-gate which affect the terminal characteristics of the MOSFET.



(a) (b)

Fig. 2.3 The band model of the symmetric DG MOSFET a) V_{gs}= 0 V b) V_{gs}= V_{th} [143].

For the symmetric double-gate device structure, at the zero gate voltage the silicon bands are flat for the mid-gap gate work function as shown in Fig. 2.3 (a). However, at V_g= V_{th}, the conduction band edge of the silicon body near the surface is bent as shown in Fig. 2.3(b) and approaches the conduction band edge

of the n+ source/drain. However, the conduction bands in both surfaces (under the front and back gates) are bent by the similar amount as the work functions of two gates are identical. At ON-state, two conductive channels are formed in the symmetric double-gate device, unless the silicon body thickness is not very thin [92].

2.3. Analysis

In this section, we have analyzed the 1-D Poisson's equation in the Cartesian coordinate system with gradual channel approximation which is given as:

$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\epsilon_{si}} e^{\frac{q(\psi - V)}{KT}} \tag{2.1}$$

where, q, ϵ_{si}, n_i, K, and T are the electron charge, dielectric permittivity of silicon, intrinsic carrier density, the Boltzmann constant, and operating temperature, respectively. V represents the quasi-Fermi potential V=0 at source side and V=V_{ds} at drain side. We have considered the n^+ DG MOSFET, therefore the hole density is negligible and the silicon film is un-doped or lightly doped that is:

$$n_b << n_i * e^{\frac{q\psi}{KT}} \tag{2.2}$$

where, n_b is the doping concentration. However, integrating (1) twice, we can get the potential distribution equation as a function of 'x' which is position in the silicon body thickness.

In the symmetric DG MOSFET, the electric field is zero at x = 0 that is the center of the silicon body thickness. The surface potential (Ψ_s) for DG MOSFET is as:

$$\psi_s = \psi_0 - \frac{2KT}{q}\left\{log\left[cos\left(\left(\sqrt{\frac{q^2 n_i}{2KT\epsilon_{si}}}\right) e^{\frac{q(\psi_0 - V)}{2KT}} x\right)\right]\right\} \tag{2.3}$$

The boundary condition for symmetric DG MOSFET:

$$\frac{\epsilon_{ox}}{t_{ox}}\left(V_{gs} - \Delta\phi_i - \psi_s\right) = \pm\epsilon_{si}\frac{d\psi}{dx}|_{x=\pm\frac{w}{2}} \tag{2.4}$$

where ε_{ox}, V_{gs} and t_{ox} are the permittivity of oxide, gate voltage and oxide thickness respectively. After solving with the help of boundary conditions, the central potential is given by:

$$\psi_0 = V + \frac{2KT}{q}\left(\ln\left(\frac{2}{at_{si}}\sin^{-1}\frac{q\epsilon_{ox}\left(V_{gs}-\psi_s\right)}{2\epsilon_{si}KTa}e^{\frac{-q\left(\psi_S-V\right)}{2KT}}\right)\right) \quad (2.5)$$

where, t_{si} is the silicon body thickness. The surface potential is given by:

$$\sin\left(a\frac{t_{s1}}{2}\sqrt{(1-\left(\frac{qc_{ox}\left(v_{gs}-\Psi\right)}{2KTe_{si}a}e^{\frac{-q\left(\Psi-V\right)}{2KT}}\right)^2}\,e^{\frac{q\left(\Psi-V\right)}{2KT}}\right) = \frac{qc_{ox}\left(v_{gs}-\Psi\right)}{2KTe_{si}a}e^{\frac{-q\left(\Psi-V\right)}{2KT}} \quad (2.6)$$

where, $a = \sqrt{\frac{q^2n_i}{2KT\varepsilon_{si}}}$ By following the Pao-Sah's dual integral [151], the drain current can be written as:

$$I_{ds} = \frac{2\pi \mathrm{W u}}{L}\int_0^{V_{ds}} Q(V)dV = \frac{2\pi \mathrm{R u}}{L}\int_{\Psi_{SS}}^{\Psi_{SL}} Q(\Psi_S)\frac{dV}{d\Psi_S}d\Psi_S \quad (2.7)$$

where, Q represents the inversion charge. Therefore, the drain current becomes:

$$I_{ds} = \frac{2\mathrm{W}C_{ox}\,\mathrm{u}}{L}\left[\begin{array}{c}\frac{2KT}{q}\left(v_g-(\Psi_{SL}-\Psi_{SS})\right)-\frac{\left(v_g-(\Psi_{SL}-\Psi_{SS})\right)^2}{4}\\ +\left(\frac{8\varepsilon_{\mathrm{si}}\,\mathrm{K}^2\mathrm{T}}{q^2WC_{ox}}\right)\ln\left(\frac{C_{ox}\left(v_g-\Psi_{SL}\right)+\frac{4e_{si}KT}{qW}}{C_{ox}\left(v_g-\Psi_{SS}\right)+\frac{4e_{si}KT}{qW}}\right)\end{array}\right] \quad (2.8)$$

where, Ψ_{SS} and Ψ_{SL} are the potential at source side (V=0) and potential on the drain side (V=V_{ds}) which can be found through equation (2.6). The total inversion charge is partitioned between the source and the drain based on Ward Dutton charge partition method as discussed in [152], is given as:

$$Q_g = \int_0^L Q(y)dy \quad (2.9)$$

$$Q_d = \int_0^L \frac{y}{L}Q(y)dy \quad (2.10)$$

$$Q_s = \int_0^L \left(1-\frac{y}{L}\right)Q(y)dy \quad (2.11)$$

where, Q_g, Q_d and Q_s are the gate charge, drain charge and source charge respectively. For the analytical expressions of the terminal charges the y is transformed to Ψ_S. Based on these expressions, the capacitances of the DG MOSFET are derived by using the Gauss law and given as:

$$C_{gs} = \frac{\partial Q_g}{\partial \Psi_{ss}}\frac{\partial \Psi_{ss}}{\partial V_s} \quad (2.12)$$

$$C_{gd} = \frac{\partial Q_g}{\partial \Psi_{SL}}\frac{\partial \Psi_{SL}}{\partial V_D} \quad (2.13)$$

$$C_{sd} = \frac{\partial Q_s}{\partial \Psi_{SL}} \frac{\partial \Psi_{SL}}{\partial V_D} \tag{2.14}$$

where C_{gs}, C_{gd} and C_{sd} are the gate to source, gate to drain and source to drain capacitances respectively. These capacitances are useful for circuit simulations.

2.4. Simulation Results

In this section, we have presented theoretically simulated results for symmetric DG MOSFET based on the electric potential, electron density, drain current, conductance, terminal charges and trans-capacitance.

The volume inversion effect is quite significant when the gate-source voltage is less than that of the threshold voltage. With the increase in gate voltage, the potential increases at the surface as the channel is formed on the surface and the minimum electric potential lies at center of the body $x = 0$, due to the screening of the center of the silicon body by the charges on the surface as shown in Fig. 2.4. In addition to this, the significant effect can be seen when the V_{gs} = 0.412 V and V_{gs} = 0.845 V. The volume inversion effect is significantly up to the threshold voltage, V_{th}= 0.4 V but as the gate voltage crosses the threshold voltage the surface and the center potentials are decoupled.

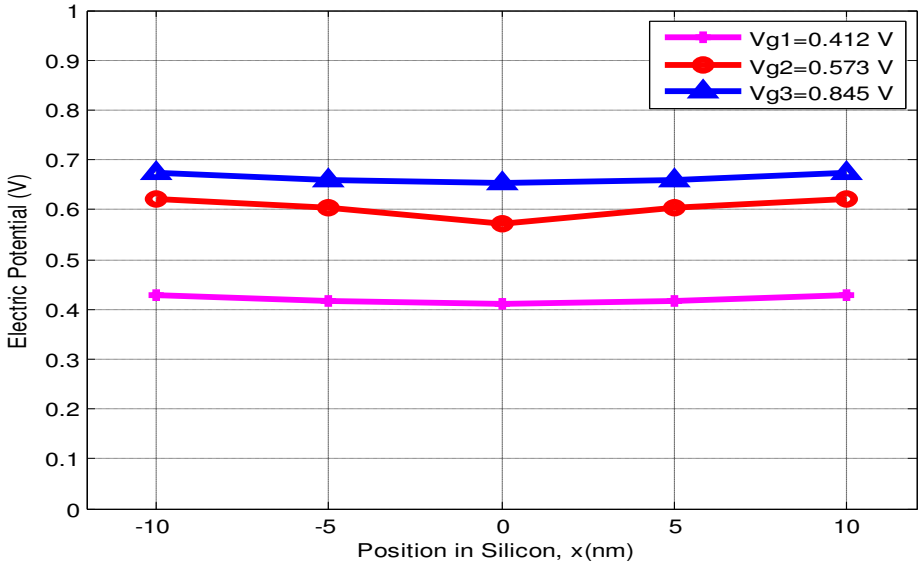


Fig. 2.4 The electric potential at various positions in the silicon body thickness (nm) at different values of the gate-source voltages.

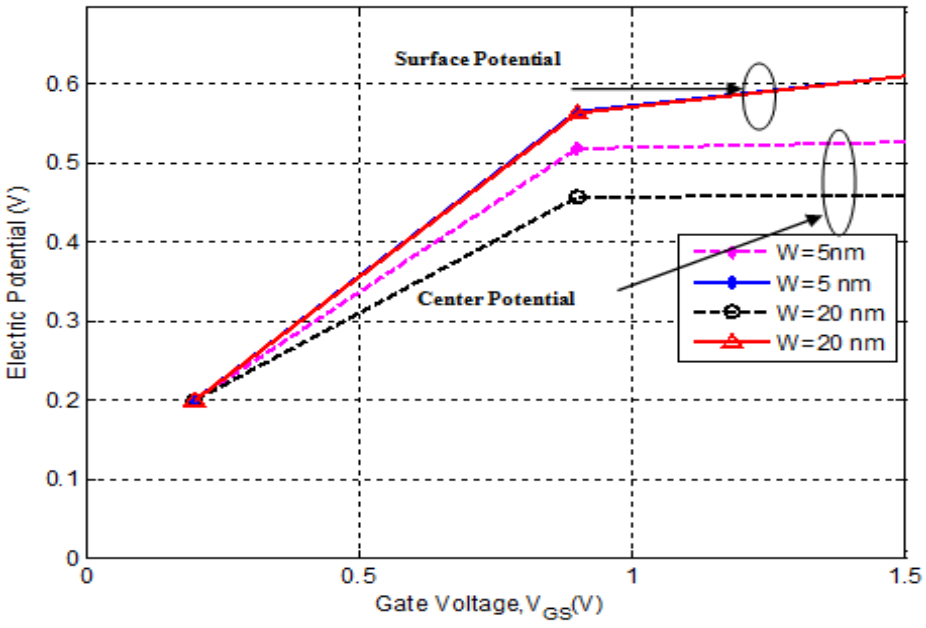
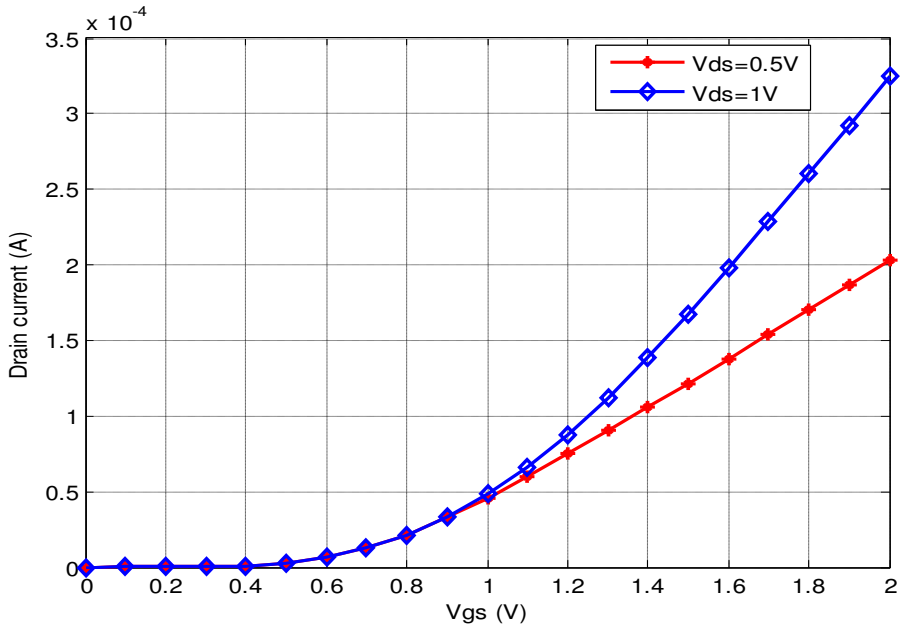
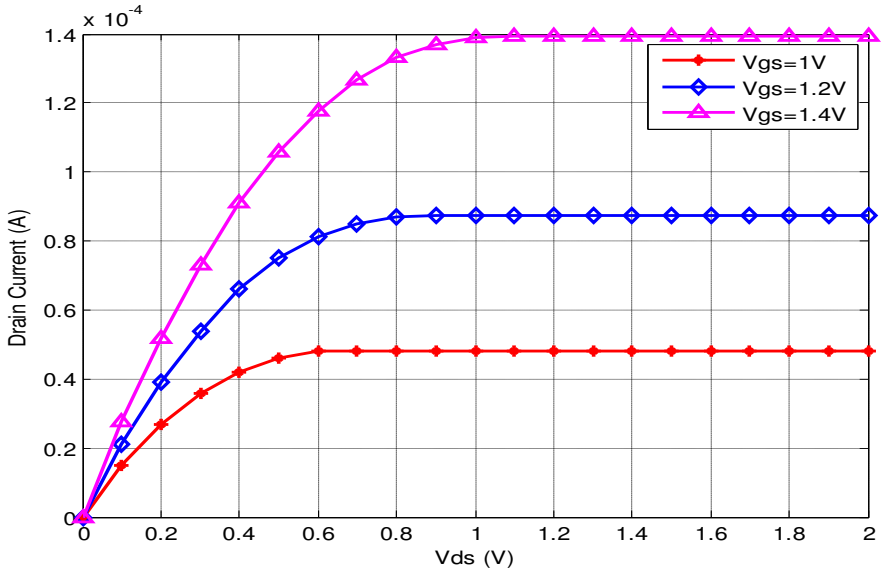


Fig. 2.5 The potential versus gate-source voltage at different body width (nm).

The center potential saturate at a specific value of potential as the arcsine argument in the equation (2.3) cannot exceed beyond $\pi/2$ but the surface potential keeps on increasing. It is illustrated through the Fig. 2.5 that the surface potential variation above the threshold voltage is independent of the silicon body thickness.



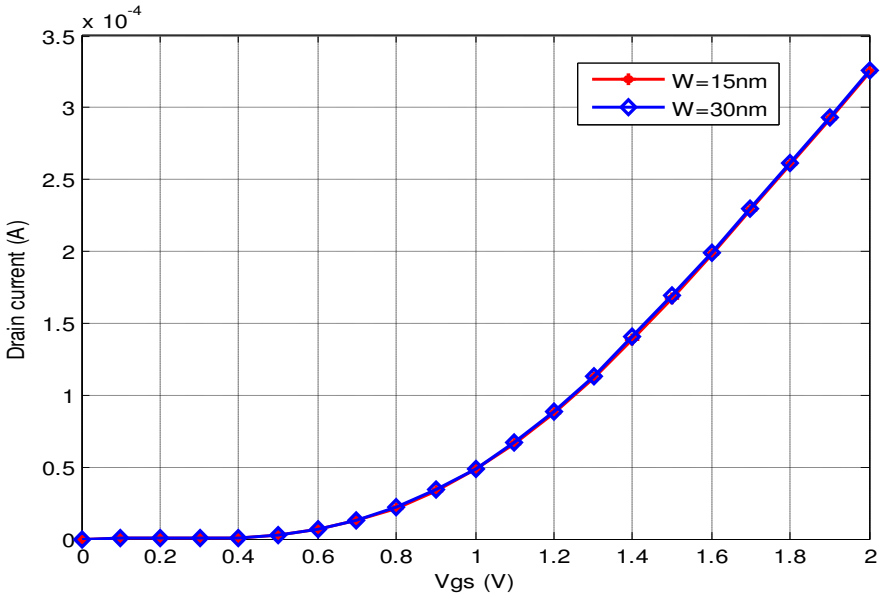
(a)



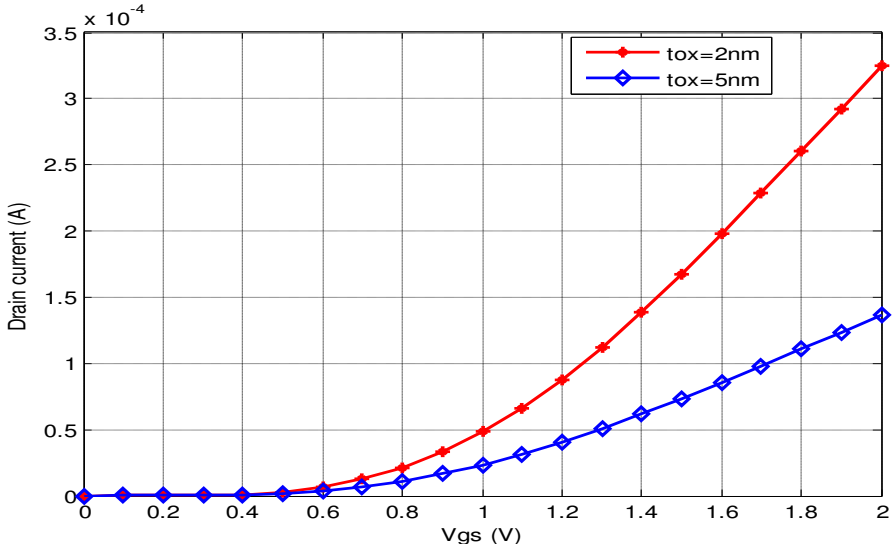
(b)

Fig. 2.6 The drain current characteristics of DG MOSFET at t_{ox} = 2 nm, W = 30 nm and L = 90 nm with (a) input characteristics and (b) output characteristics.

The input and output characteristics of the DG MOSFET as shown in Fig. 2.6(a) and (b) are similar to that of the conventional MOSFET. The response of the drain-to-source voltage, over the drain current with various values of V_{gs} as shown in Fig. 2.6(b) reveals the two operating regions i.e. linear and saturation regions.



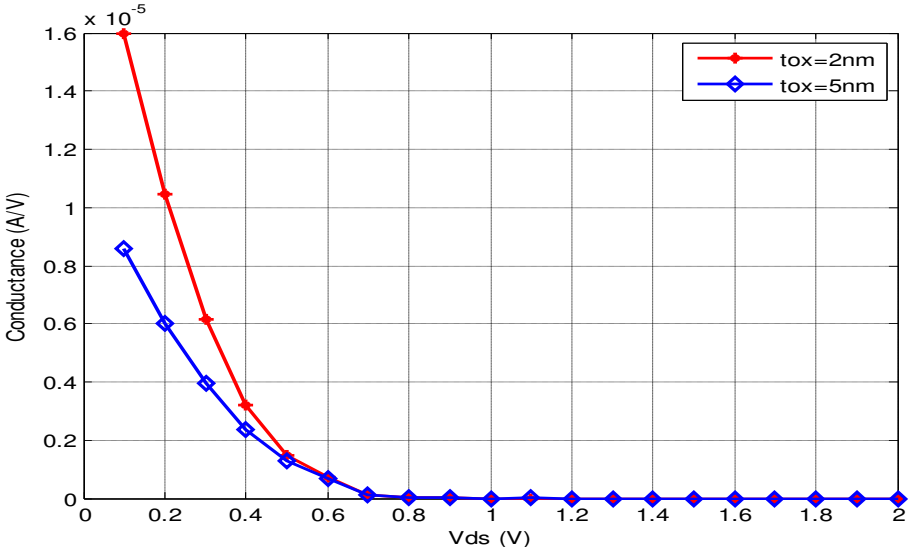
(a)



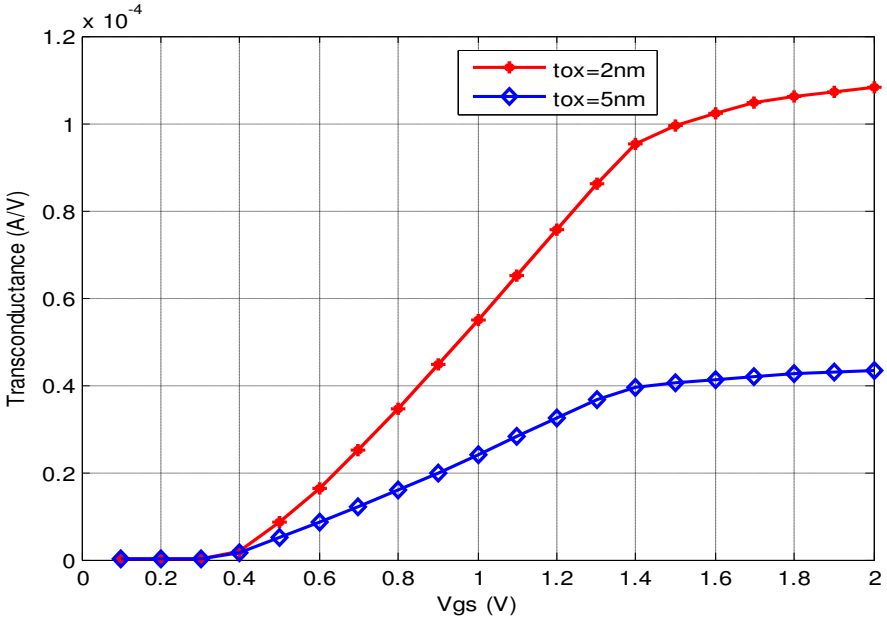
(b)

Fig. 2.7 The response of gate-to-source voltage, over the drain current with V_{ds} = 1V and L = 90 nm for different values of (a) device width with fixed t_{ox}= 2 nm and (b) oxide thickness with fixed W = 30 nm.

On interpolating the curves of Fig. 2.6(a) on the x-axis the value of threshold voltage can be interpreted as V_{th}= 0.6 V and V_{th}= 0.7 V for V_{ds}=0. 5 V and V_{ds}=1 V, respectively. The drain current is independent of the device width Fig. 2.7 (a), however, its dependence over the oxide thickness is quite significant as shown in Fig. 2.7 (b).



(a)

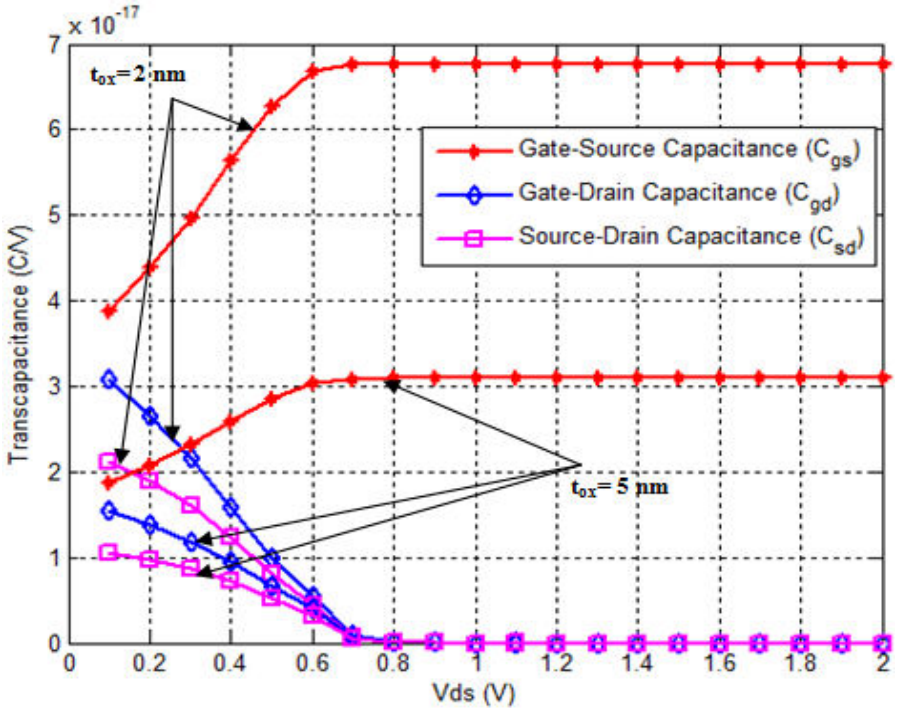


(b)

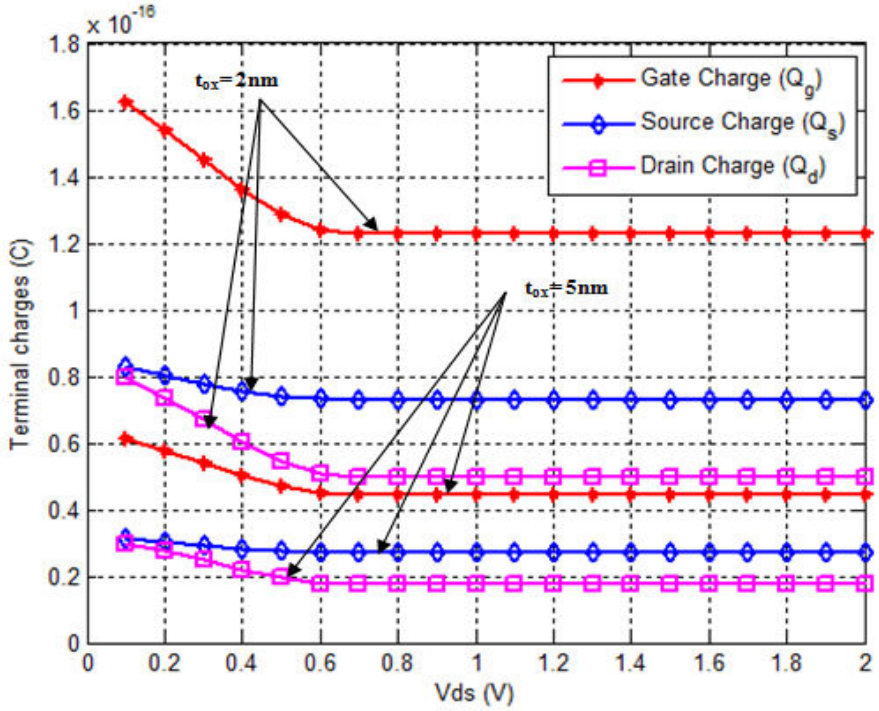
Fig. 2.8 The effect of oxide thickness on the (a) conductance with V_{gs}= 1 V and (b) trans-conductance with V_{ds}= 1 V.

It is well illustrated in Fig. 2.7(b), that the charge formation on the surface, increases with the reduction in the oxide thickness and results the increase in the current formation of the device. Fig. 2.8 shows the variation of oxide thickness on the conductance and trans-conductance for W = 30 nm and L = 90 nm of DG MOSFET. As the drain-to-source voltage increases for chosen oxide thickness, the conductance of the device decreases and reduces to zero as the pinch-off point is achieved as shown in Fig. 2.8(a). In addition to this, with the decrease of oxide thickness, the conductance of the device increases. In Fig. 2.8(b) as the gate voltage reaches the threshold voltage the trans-conductance achieves its highest peak value and reduces after threshold voltage. However, with the increase of the oxide thickness, the trans-conductance decreases and results the significant enhancement in the overall gain of the device. In Fig. 2.9(a) and Fig. 2.9(b) illustrates the trans-capacitance and the terminal charges variation with V_{ds} for a specific value of the oxide thickness. As the oxide thickness increases, the charge storage capacity decreases, which further results in the decrease in capacitance of

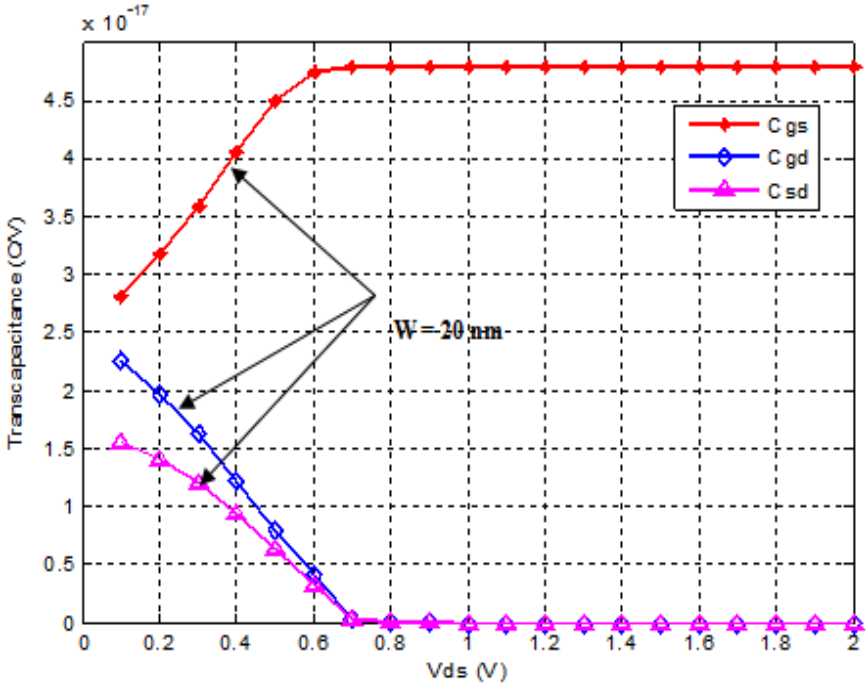
the device. However, the gate-drain capacitance (C_{gd}) and the source-drain capacitance (C_{sd}) are not coupled to drain voltage after the saturation is achieved.



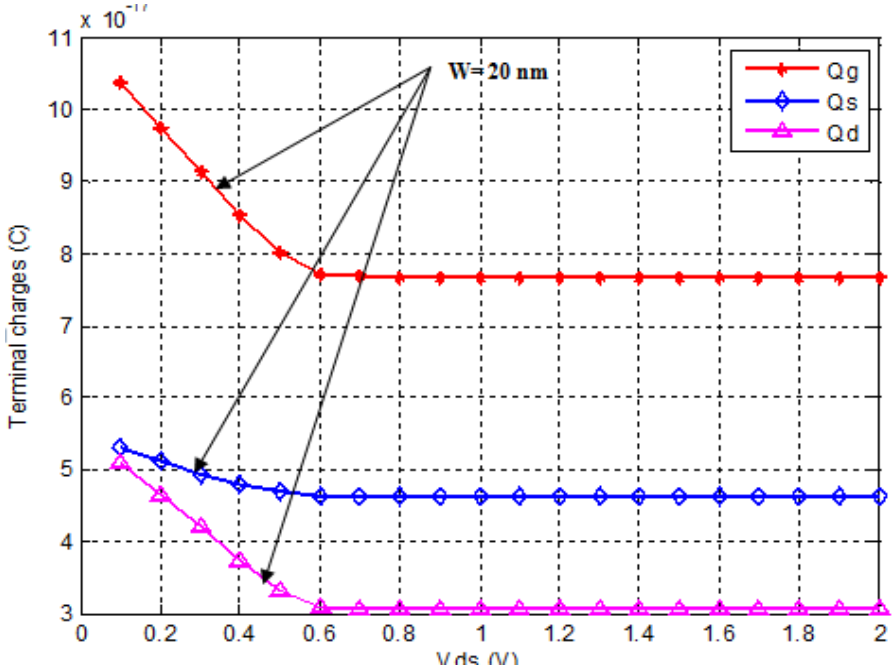
(a)



(b)



(c)



(d)

Fig. 2.9 The response of the drain-to-source voltage on the (a) trans-capacitance, (b) terminal charges with $W = 30$ nm and $L = 90$ nm, (c) trans-capacitance and (d) terminal charges with $W = 20$ nm, $t_{ox} = 2$ nm and $L = 90$ nm at $V_{gs} = 1$.

Fig. 2.9(c) and Fig. 2.9(d), where t_{ox}= 2 nm W = 20 nm shows the variation with a width of the device (W). When comparing with Fig. 2.9(a) and Fig. 2.9 (b) with these, it is observed that as the width reduces the terminal charges and the trans-capacitance also reduces due to the lesser area of the device. It is illustrated by Fig. 2.9(b) and Fig. 2.9(d) that the source charge always saturate to the value of 6/10 of the gate charge and drain the charge saturate to 4/10 of the gate charge.

2.5. Summary

The analytical surface potential based current voltage modelling of a symmetric DG MOSFET with un-doped silicon body is presented. The results reveal that for the symmetric DG MOSFET the electric potential varies in proportion with the gate voltage and the minimum potential lies at the center of the silicon body due to the symmetric nature of the device. In addition to this, the volume inversion effect is also significant and the surface potential variation beyond the threshold voltage is independent of the silicon body thickness. The I-V and C-V model are also reproduced and it is seen that the drain current in the strong inversion region is invariant to a width of the device.

CHAPTER 3

PERFORMANCE ANALYSIS OF UNDOPED AND GAUSSIAN-DOPED SURROUNDING-GATE MOSFET

3.1. Introduction

In additions to certain advantages [153, 154], the DG MOSFET has certain limitations such as, identical sized gates, self-alignment of the source and drain regions to both top and bottom gates, and alignment of the two gates with one another [11] which make DG MOSFET an inferior candidate for CMOS technology. Ernst et al [155] have also reported the degradation of the mobility of the double gate MOSFET. Therefore, for the further advancement, the channel can completely surround by the gate that is the surrounding gate MOSFET which increases the gate control of the channel and reduces the SCE's [144, 156]. Liu et al. [157] have derived a charge based model applicable to both the intrinsic and heavily doped body surrounding gate MOSFET based on the concept of threshold voltage. In addition to this, various literatures [158-160] are available for the reduction of energy carriers that are a consequence of the high electric field density [161], with the help of gate engineering. Moreover, the halo doping in the device and the junction-less surrounding gate MOSFET structure is also very helpful in diminishing the SCE [162-164]. Furthermore, the actual doping profile relevant to the fabrication of devices is the Gaussian doping, which also has not been analyzed to date.

3.2. Structure Description

For the cylindrical surrounding gate MOSFET, the silicon pillar of radius R is surrounded by the gate in a cylindrical fashion as shown in Fig. 3.1. The structure significantly increases the electrostatic gate control over the channel and this

structure is effective for shielding the drain electric field-lines from reaching the source to reduce the potential barrier as well as reducing the SCE.

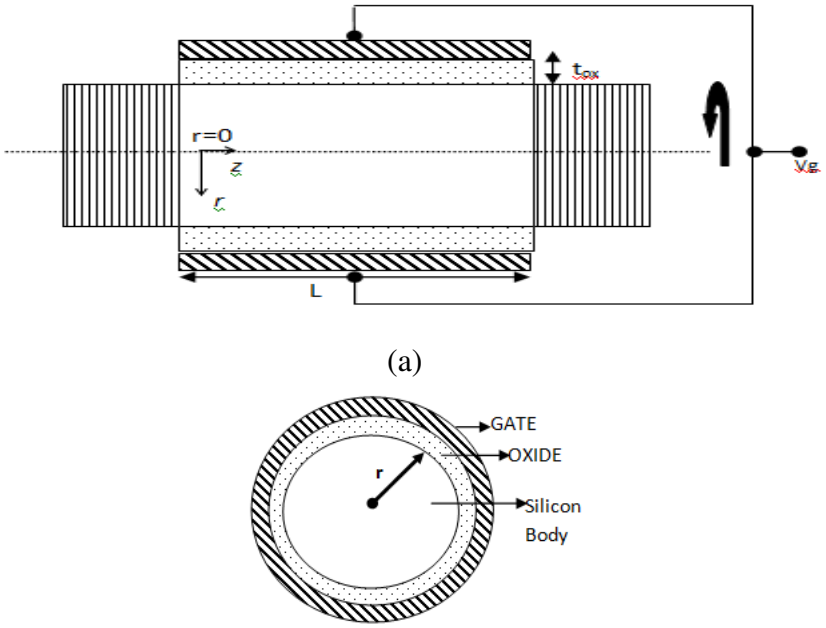


Fig. 3.1 The surrounding gate MOSFET (a) 2-D longitudinal cross-sectional view and (b) horizontal cross-sectional view.

Due to un-doped/lightly doped body, the problem of random dopant fluctuation is also absent.

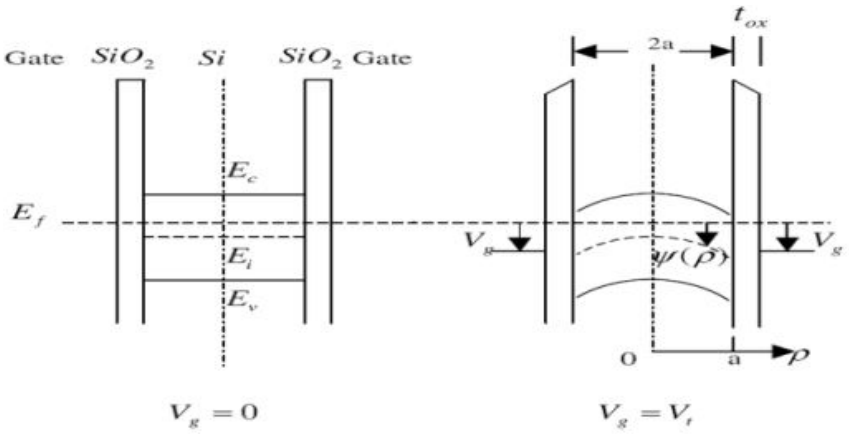


Fig. 3.2 The energy band diagram of surrounding gate MOSFET (a) at V_{gs} = 0 V and (b) $V_{gs} = V_{th}$.

The silicon energy bands are flat without any applied gate voltage as shown in Fig. 3.2 (a). However, when the gate voltage is applied and it equals to the threshold voltage ($V_g = V_{th}$), the conduction band edge of the silicon body near the surface is bent and approaches the conduction band edge of the n+ source/drain [165].

3.3. Analysis

3.3.1. Undoped Body Surrounding-Gate MOSFET

3.3.1.1. Surface Potential

For the analysis of surrounding gate MOSFET, the Poisson's equation in cylindrical coordinate system is solved with the assumptions of gradual channel approximation (i.e. neglecting the lateral field term:

$$\frac{d^2\Psi}{dr^2} + \frac{1}{r}\frac{d\Psi}{dr} = \frac{q^2 n_i}{\varepsilon_{si} kt} e^{\frac{q(\Psi - V)}{KT}} \tag{3.1}$$

where, q, ε_{si}, n_i, K, and T are the electron charge, dielectric permittivity of silicon, intrinsic concentration of silicon, the Boltzmann constant and the absolute working room temperature, respectively. V is the quasi-Fermi potential whose value $V = 0$ and $V = V_{ds}$ at the source and drain side, respectively. As we have considered the n^+ surrounding gate MOSFET, therefore the hole density is negligible. In addition to this, the silicon film is un-doped or lightly doped. The Equation (1) is solved by the method of transformation of variable and the solution is given as:

$$\Psi(r) = A - \frac{2KT}{q} \ln\left(1 - \left(\frac{q^2 n_i}{\varepsilon_{si} KT} e^{\left(\frac{q}{KT}(A - V)\right)} r^2\right)\right) \tag{3.2}$$

where, A is the integration constant or the center potential whose value has to be achieved with the help of boundary conditions as follows:

$$\frac{d\Psi}{dr}\Big|_{r=0} \tag{3.3}$$

$$\Psi(r = 0) = A = \Psi_0 \tag{3.4}$$

$$\Psi(r = R) = \Psi_S \tag{3.5}$$

The solution must also satisfy the Gauss law which is given as:

$$c_{ox}\left(v_{gs}-\Psi\right)=\varepsilon_{\mathrm{si}}\frac{\mathrm{d}\Psi}{\mathrm{dr}}|_{\mathrm{r=R}} \tag{3.6}$$

By solving (3.2) and (3.6), the center potential and surface potential can be given as:

$$\Psi_0=2V-\Psi_S+\frac{2KT}{q}\ln\left(\frac{2c_{ox}}{Rn_iq}\left(v_{gs-}-\Psi_S\right)\right) \tag{3.7}$$

$$\left(v_{gs}-\Psi_S\right)\left[\frac{1}{R}+\frac{qc_{ox}}{4esiKT}\left(v_g-\Psi_S\right)\right]=\frac{qn_i}{2c_{ox}}e^{\frac{q}{KT}(\Psi_S-V)} \tag{3.8}$$

The equation (3.8) can be solved iteratively and Ψ_S can have multiple numbers of roots and accurate value has to be guessed. The inversion charge density (Q) of the structure is given by:

$$Q=c_{ox}\left(v_{gs}-\Psi_S\right) \tag{3.9}$$

3.3.1.2. Drain Current, Terminal Charge and Trans-Capacitance Modelling

The equation (3.8) is required for the current and the charge modelling. By using the current continuity equation:

$$I_{ds}=A\square Q\frac{dV}{dy} \tag{3.10}$$

where, A, Q, and μ are the area of the cylinder, inversion charge, and mobility, respectively, and following the Pao-Sah's dual integral [151] drain current can be written as:

$$I_{ds}=\frac{2\pi\mathrm{R}\square}{L}\int_0^{V_{ds}}Q(V)dV=\frac{2\pi\mathrm{Ru}}{L}\int_{\Psi_{SS}}^{\Psi_{SL}}Q(\Psi_S)\frac{dV}{d\Psi_S}d\Psi_S \tag{3.11}$$

where, Ψ_{SS} and Ψ_{SL} are the surface potential at the source side (V = 0) and drain side ($V = V_{ds}$), respectively, and the relation between the quasi-Fermi potential can be obtained by the differentiating (3.8). However, performing the integration of the (3.11) analytically the drain current of the surrounding gate MOSFET:

$$I_{ds}=\frac{2\pi\mathrm{R}c_{ox}\,\mathrm{u}}{L}\left[\begin{array}{c}\left(v_{gs}+\frac{2KT}{q}\right)(\Psi_{SL}-\Psi_{SS})-\frac{\left(\Psi_{SL}{}^2-\Psi_{SS}{}^2\right)}{2}\\+\left(\frac{4\varepsilon_{\mathrm{si}}\mathrm{K}^2\mathrm{T}^2}{q^2RC_{ox}}\right)\ln\left(\frac{\frac{1}{R}+\frac{qC_{ox}}{4e_{si}KT}\left(v_{gs}-\Psi_{SL}\right)}{\frac{1}{R}+\frac{qC_{ox}}{4e_{si}KT}\left(v_{gs}-\Psi_{SS}\right)}\right)\end{array}\right] \tag{3.12}$$

The trans-conductance and conductance of MOSFET are the important parameters governing the AC characteristics of the particular MOSFET. Moreover, it also decides the current driving capabilities of the MOSFET. The trans-conductance (G_m) of the device tells about the variation of the drain current with the input voltage i.e. gate-to-source voltage.

$$G_m = \frac{\partial I_D}{\partial V_{gs}} = \frac{\partial I_D}{\partial \Psi_S}\frac{\partial \Psi_S}{\partial V_{gs}} \tag{3.13}$$

Similarly, the output conductance tells about the change in the drain current with the output voltage i.e. drain-to-source voltage:

$$G_{ds} = \frac{\partial I_D}{\partial V_{ds}} = \frac{\partial I_D}{\partial \Psi_S}\frac{\partial \Psi_{SS}}{\partial V_{ds}} \tag{3.14}$$

For the modelling of quasi-terminal charges Ward Dutton charge partition method [152] is used where the total inversion charge given by (3.9) is partitioned into source part and drain part.

$$Q_g = \int_0^L Q(y)dy \tag{3.15}$$

$$Q_d = \int_0^L \frac{y}{L} Q(y)dy \tag{3.16}$$

$$Q_s = \int_0^L \left(1 - \frac{y}{L}\right) Q(y)dy \;\; = \;\; Q_g - Q_d \tag{3.17}$$

where, Q_g, Q_d, and Q_s are the gate charge, drain charge and source charge, respectively. Moreover, we are modelling the charges based on the surface potential, therefore transforming y to Ψ_S in all the equations and then performing the integration analytically and yield the expressions on the terminal charges. However, based on the expressions of the terminal charges, the capacitances of the surrounding gate MOSFET are also derived by using:

$$C_{gs} = \frac{\partial Q_g}{\partial \Psi_{ss}}\frac{\partial \Psi_{ss}}{\partial V_s} \tag{3.18}$$

$$C_{gd} = \frac{\partial Q_g}{\partial \Psi_{SL}}\frac{\partial \Psi_{SL}}{\partial V_D} \tag{3.19}$$

$$C_{sd} = \frac{\partial Q_s}{\partial \Psi_{SL}}\frac{\partial \Psi_{SL}}{\partial V_D} \tag{3.20}$$

where, C_{gs}, C_{gd} and C_{sd} are the gate-to-source capacitance, gate-to-drain capacitance and source-to-drain capacitance, respectively. These capacitances are useful for circuit simulations.

3.3.2. Gaussian Doping

As the device dimension approaches towards the nano-scale regime, the reduction of threshold voltage is observed, therefore for the requirement of its adjustment, the doping must be needed. The uniform channel doping is not the practical form due to a large number of ion implantation stages required during the fabrication process [166, 167]. Thus, the analysis of non-uniform doping in the surrounding gate MOSFET is vital for the accurate device performance. Therefore, for the analysis of non-uniform doping in the device, the Gaussian distribution function is used and the Poisons equation is given as:

$$\frac{d^2\Psi}{dr^2} + \frac{1}{r}\frac{d\Psi}{dr} = \frac{Qq}{\sqrt{2\pi}\sigma\varepsilon_{si}} e^{-\left(\frac{r-R_p}{\sqrt{2}\sigma}\right)^2} \tag{3.21}$$

where Q is the implantation dose per unit area at a projected range R_p with straggle $\boldsymbol{\sigma}$. As per the authors knowledge, there is no closed form solution exists for the equation (3.21), therefore, based on the approximation of the Taylor series expansion of the exponential and error function, the solution of the Gaussian doped surrounding gate MOSFET can be presented as:

$$\Psi_s = A - \frac{2KT}{q}\ln\left(1 - \left(\frac{q^2 n_i}{\varepsilon_{si} KT} e^{\left(\frac{q}{KT}(A-V)\right)} R^2\right)\right) + \frac{Qq}{\sqrt{2\pi}\sigma\varepsilon_{si}}(x) \tag{3.22}$$

where the second term (right-hand side) of Equation (32) represents the potential due to mobile charge and the third term represents the potential due to the Gaussian doping. The term x in (3.22) is given on the next page. The approximation is valid only for those values of R_p and $\boldsymbol{\sigma}$ for which the below condition is satisfied:

$$0 < \frac{r-R_p}{\sqrt{2}\sigma} < 1 \tag{3.23}$$

After solving equation (3.22) with the appropriate boundary condition equation (6) the center (Ψ_0) and the surface potential (Ψ_s) can be given as:

$$\Psi_0 = V + \frac{KT}{q}\ln\frac{C_{ox}\left(V_{gs}-\Psi_s\right)+\frac{Qq}{\sqrt{2\pi}\sigma}(y)}{\frac{Rq\,n_i}{2}+\frac{n_i q^2 R^2}{8\varepsilon_{si}KT}\left(C_{ox}\left(V_{gs}-\Psi_s\right)+\frac{Qq}{\sqrt{2\pi}\sigma}(y)\right)} \tag{3.24}$$

$$\frac{C_{ox}\left(V_{gs}-\Psi_s\right)+\frac{Qq}{\sqrt{2\pi}\sigma}(y)}{\frac{Rq\,n_i}{2}+\frac{n_i q^2 R^2}{8\varepsilon_{si}KT}\left(C_{ox}\left(V_{gs}-\Psi_s\right)+\frac{Qq}{\sqrt{2\pi}\sigma}(y)\right)} =$$

$$\left(1-\frac{n_i q^2}{8\varepsilon_{si}KT}R^2\left(\frac{C_{ox}\left(V_{gs}-\Psi_s\right)+\frac{Qq}{\sqrt{2\pi}\sigma}(y)}{\frac{Rq\,n_i}{2}+\frac{n_i q^2 R^2}{8\varepsilon_{si}KT}\left(C_{ox}\left(V_{gs}-\Psi_s\right)+\frac{Qq}{\sqrt{2\pi}\sigma}(y)\right)}\right)\right)^2 e^{\frac{q}{KT}\left(\Psi_s-V-\frac{Qq}{\sqrt{2\pi}\sigma\varepsilon_{si}}(x)\right)} \tag{3.25}$$

where,

$$x = -\frac{R^2 {R_p}^2}{8\sigma^2}-\frac{R^3 {R_p}^3}{18\sigma^4}-\frac{R^5 R_p}{50\sigma^4}+\frac{R^3 R_p}{9\sigma^2}+\frac{R^2}{4}+\frac{3R^4 {R_p}^2}{64\sigma^4}+\frac{R^6}{288\sigma^4}-\frac{R^4}{32\sigma^2}+\frac{R^2 {R_p}^4}{32\sigma^4} \tag{3.26}$$

$$y = -\frac{R{R_p}^2}{4\sigma^2}-\frac{R^2 {R_p}^3}{6\sigma^4}-\frac{R^4 R_p}{10\sigma^4}+\frac{R^2 R_p}{3\sigma^2}+\frac{R}{2}+\frac{3R^3 {R_p}^2}{16\sigma^4}+\frac{R^5}{48\sigma^4}-\frac{R^3}{8\sigma^2}+\frac{R{R_p}^4}{16\sigma^4} \tag{3.27}$$

3.4. Numerical Results and Discussion

In this section, we have presented the numerically simulated results of the surrounding gate MOSFET based on the potential distribution, inversion charge, drain current, terminal charges and the trans-capacitance. In addition to this, the Gaussian doping analysis is also performed.

3.4.1. Undoped Body Surrounding gate MOSFET Analysis

3.4.1.1. Potential Analysis

When the V_{gs} is less than that of the V_{th}, the volume inversion effect is quite significant (V_{gs} = 0.135 V and V_{gs} = 0.435 V) and the potential is constant across the radius of the cylinder, but at the gate-source voltage exceeds the threshold voltage (V_{gs}= 0.558 V) the potential at the surface side increases as compared to the center potential due to the formation of a channel on the surface of the device which is shown in Fig. 3.3.

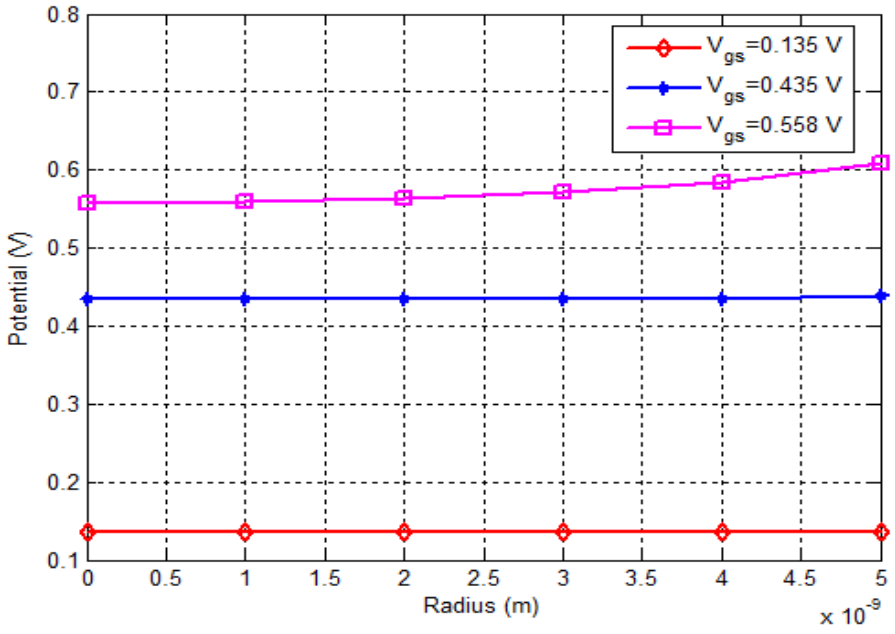
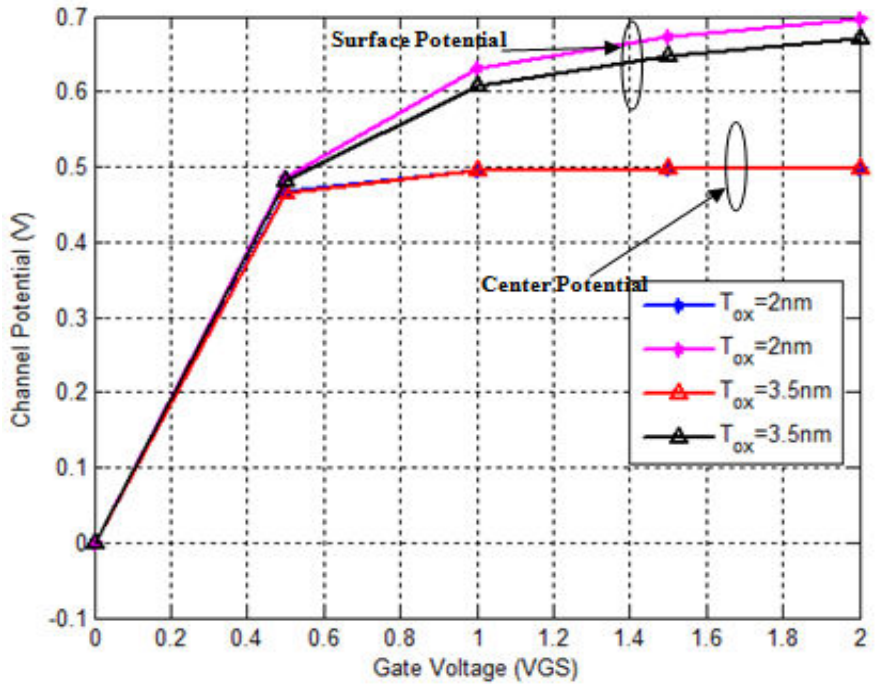
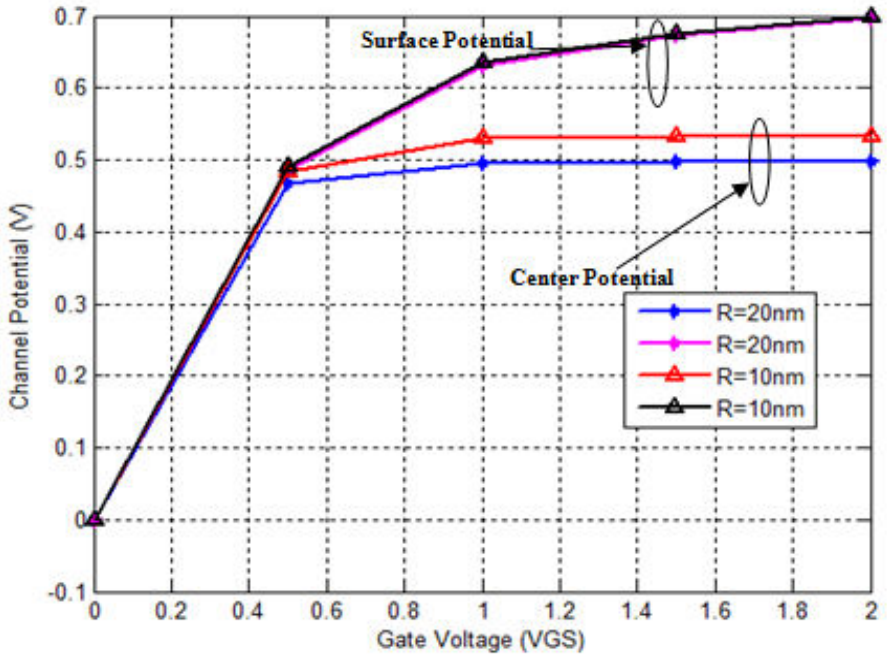


Fig. 3.3 The potential versus radius of the cylinder (*R*) with different values of gate-to-source voltage (V_{gs}).



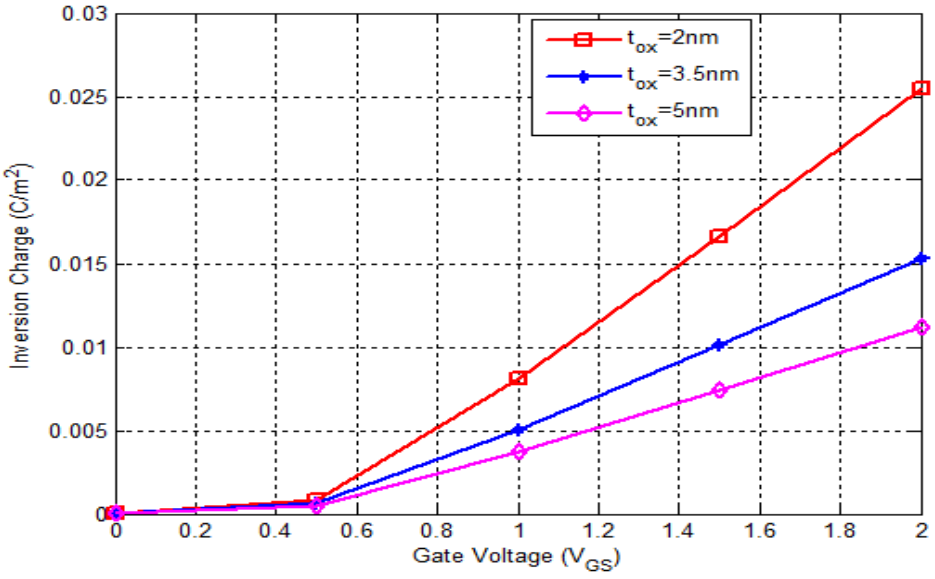
(a)



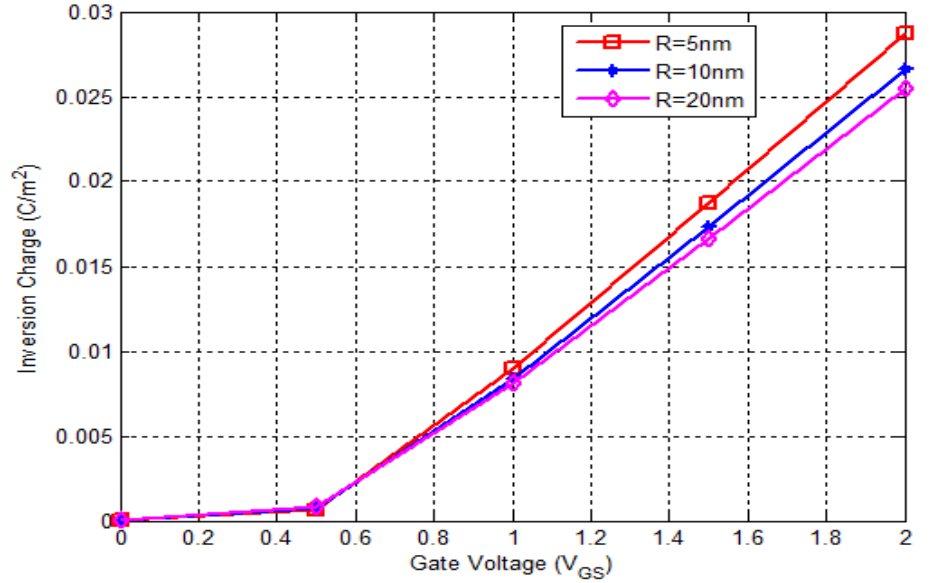
(b)

Fig. 3.4 The response of the gate-to-source voltage (V_{gs}) over surface potential and center potential with variation in the (a) oxide thickness (t_{ox}) and (b) radius of the cylinder (R).

Figure 3.4(a) depicts the variation of center potential and surface potential with the variation of the V_{gs} for different values of t_{ox}. The saturation in the center potential is seen as the gate voltage increases due to the channel formation at the surface which hinders the electric field lines to pass through it. On the other hand, the surface potential keeps on increasing with the gate-to-source voltage as the carriers in the channel keep on increasing. The center potential for both the oxide thicknesses (t_{ox}) saturates at the same point, which reveals that the center potential is un-affected by the variation of the oxide thickness as shown in Fig. 3.4(a). Fig. 3.4(b) shows the variation of the center and the surface potential with different values of R. The variation in R affects the center potential significantly more compared to that of the surface potential, as the central portion of the device is at the longer distance from the gate, therefore for the higher value of R, the central potential is significantly low.



(a)

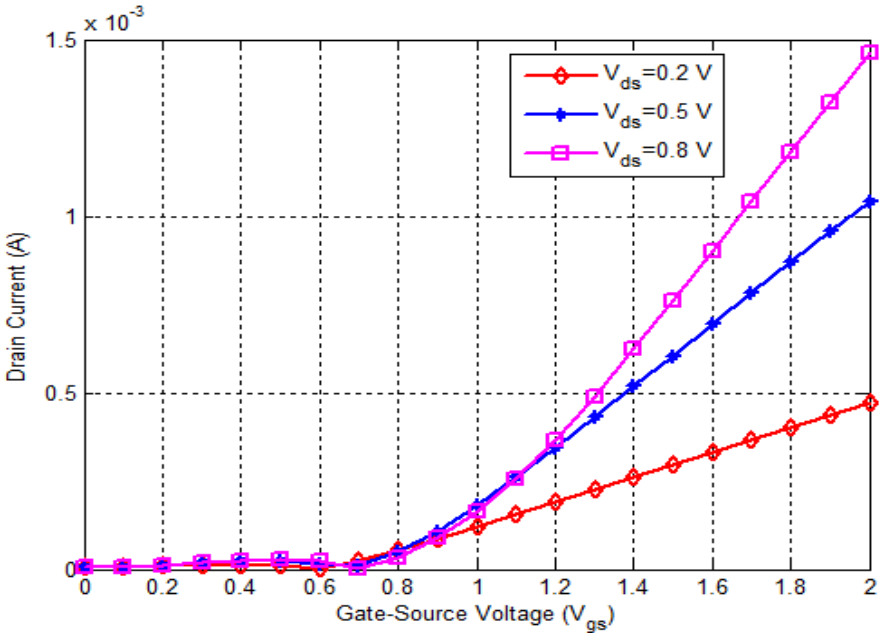


(b)

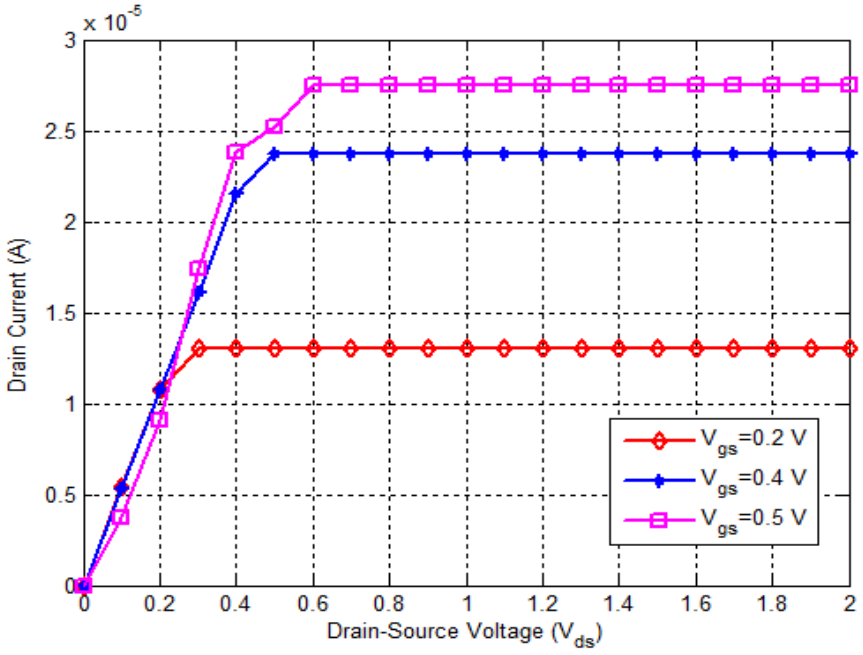
Fig. 3.5 The response of gate-to-source voltage (V_{gs}) over the inversion charge with the variation of (a) oxide thickness (t_{ox}) and (b) radius of the cylinder (R).

For the smaller value of t_{ox}, the more electric field is generated at the surface which further increases the inversion charge as revealed from Fig. 3.5(a). Fig. 3.5(b) shows the variation of inversion charge with different radius, which is very small due to the charge accumulation on the surface.

3.4.1.2. Drain Current, Terminal Charges and Trans-Capacitance Analysis



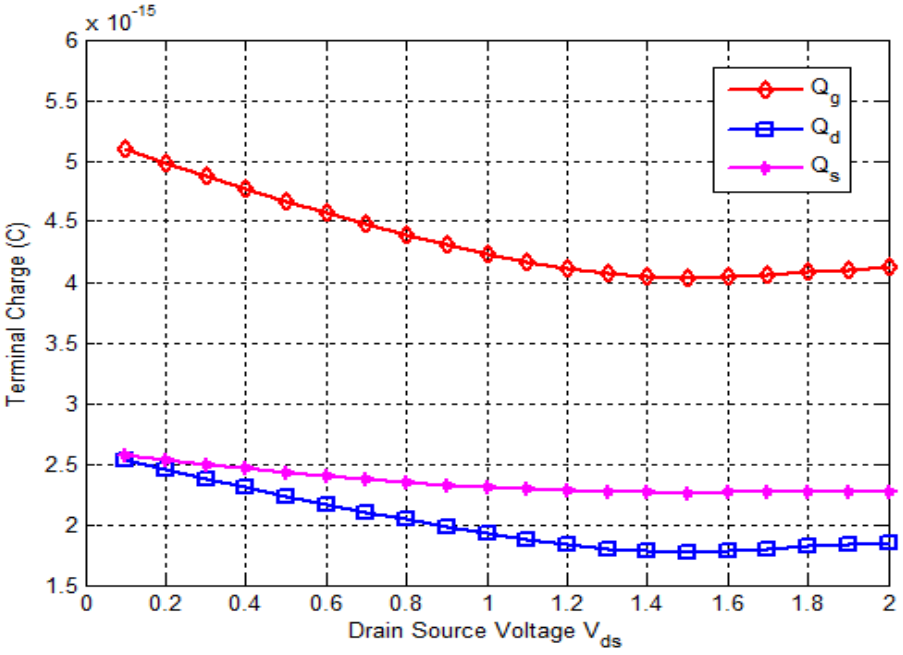
(a)



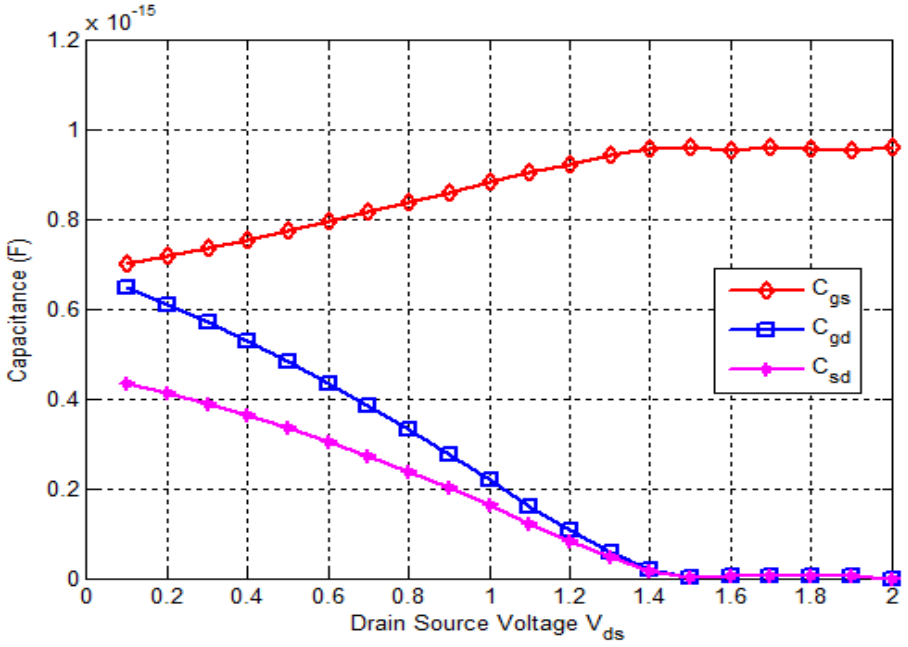
(b)

Fig. 3.6 The drain current characteristics of the surrounding gate MOSFET with t_{ox} = 2 nm, R = 20 nm and L = 50 nm with the (a) gate-to-source voltage (V_{gs}) and (b) drain-to-source voltage (V_{ds}).

The input and the output characteristics of the surrounding gate MOSFET is presented in Fig. 3.6. However, on interpolating the curves of Fig. 3.6(a) on the x-axis i.e. gate-to-source voltage (V_{gs}), the threshold voltage can be extracted. Similarly, as the gate-to-source voltage increases, the drain current also increases and different operating regions are observed which are analogous to that of the conventional MOSFET as shown by Fig. 3.6(b). When the saturation is achieved, i.e. V_{gs} = 1.5 V, the charge in device also saturates to some extent as shown in Fig. 3.7(a). However, it is observed that the source charge saturates to 6/10 and drain charge saturates to 4/10 of the saturated value of gate charge, respectively. In addition to this, a sharp decrease in the gate charge with V_{ds} is presented in Fig. 3.7(a). In Fig. 3.7(b), the variation of capacitance with the drain-to-source voltage for V_{gs} = 2 V, R = 20 nm and t_{ox} = 2 nm is illustrated. Due to the decrease in the drain terminal charges, the drain related trans-capacitance decreases, however, as for higher V_{ds}, significantly more current is formed in the device which increases the gate-source related trans-capacitance due to increase in the movement of number of charge from source-to-drain.



(a)



(b)

Fig. 3.7 For the fixed $V_{gs} = 2$ V the (a) variation of the charge with drain-to-source voltage, and (b) variation of the capacitance with the drain-to-source voltage.

However, after the device drain current saturation, the capacitance also saturates, which is observed at $V_{ds} = 1.5$ V in Fig. 3.7(b).

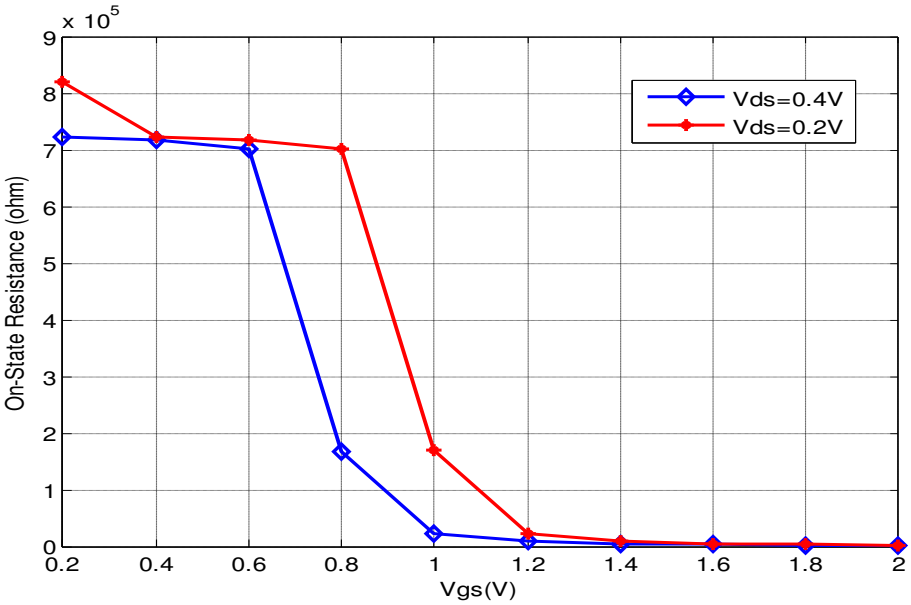


Fig. 3.8 The on-state resistance versus gate-to-source voltage (V_{gs}) for different drain-to-source voltage.

Fig. 3.8 demonstrate the variation of the on-state resistance with the variation of the V_{gs} for different values of the V_{ds}. Initially, the channel resistance is very high, but as the gate voltage increases towards the threshold voltage, due to the formation of the channel on the surface the resistance decreases. It is seen in the Fig. 3.8 that the resistance remains constant for a short period of time which shows the volume inversion effect quite significant in the device.

3.4.2. Gaussian Doping Analysis

In this section, the Gaussian doping is analyzed for the chosen dimensions of the device such as: R = 20 nm, t_{ox} = 2 nm, L = 50 nm, R_p = 17 nm and $\boldsymbol{\sigma}$ = 15 nm.

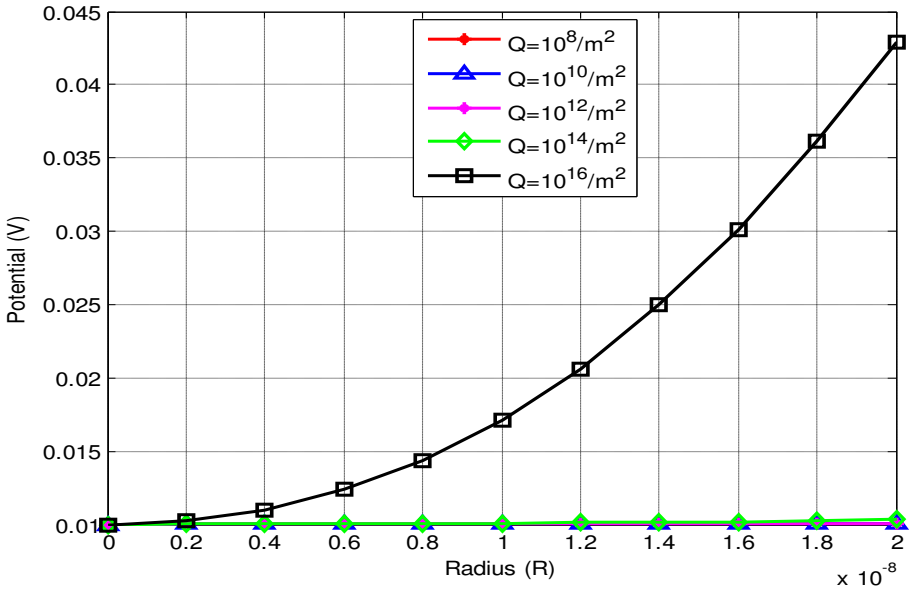


Fig. 3.9 The variation of body potential across the radius of cylinder (R) with different implantation doses.

Fig. 3.9 shows the variation of the potential across the radius of the cylinder (R) with a various implanted dose per unit area (Q) for the fixed gate-to-source voltage (V_{gs}=0.01).

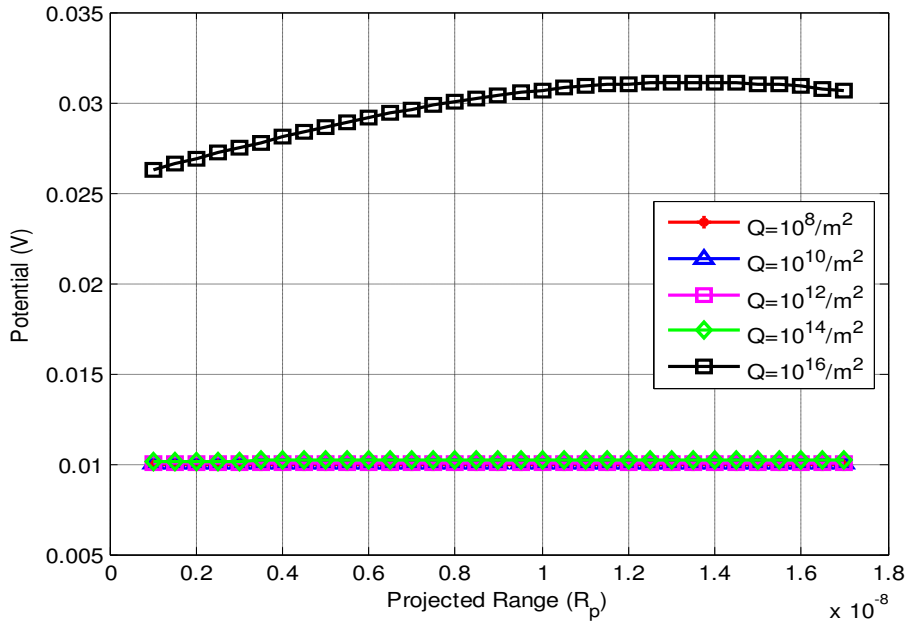


Fig. 3.10 The variation of body potential across the projected range (R_p) with different implantation doses.

As the doping increases, the threshold voltage of the surrounding gate MOSFET reduces and the operation of the device can be performed even at low voltages, as the inversion can take place at low gate voltage. The significant effect of doping can be seen when the $Q = 10^{16}/m^2$ below which inversion layer would not be strong enough for the conduction. Fig. 3.10 illustrates the variation of body potential across the projected range (R_p) with a various implanted dose (Q). The body potential follows the parabolic path across the variation of the projected range parameter (R_p). However, the appropriate value of $Q = 10^{16}/m^2$, below which the body potential of the device remains constant. The response of gate-to-source voltage (V_{gs}) on center and the surface potential are similar to that of the un-doped surrounding gate MOSFET as shown in Fig. 3.11. However, the center potential does not vary with the doping dose, but a significant increase in the surface potential is observed at $Q = 10^{16}/m^2$ which would be effective for the increase in the drain-current for the device.

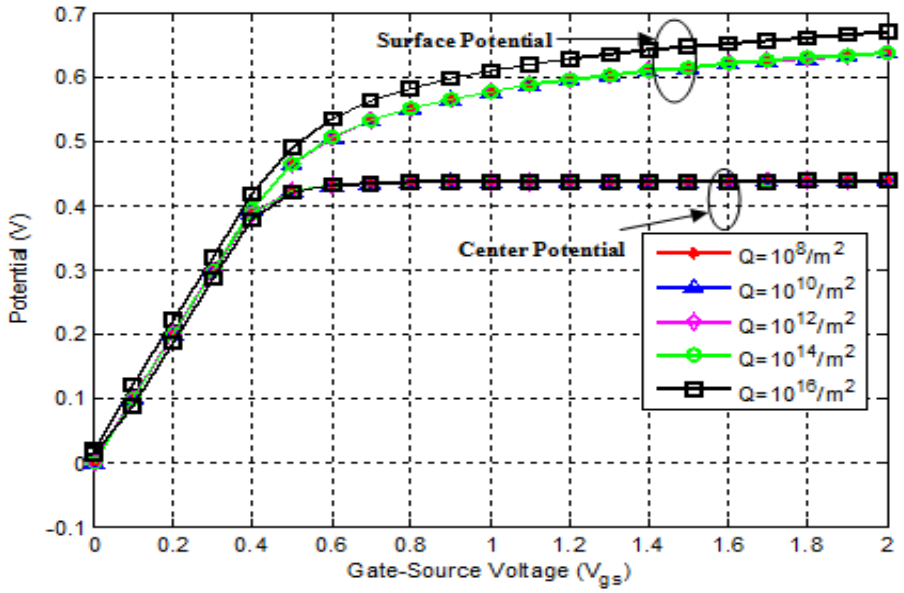


Fig. 3.11 The response of gate-to-source voltage (V_{gs}) on the potential (center and surface) with different implantation doses (Q).

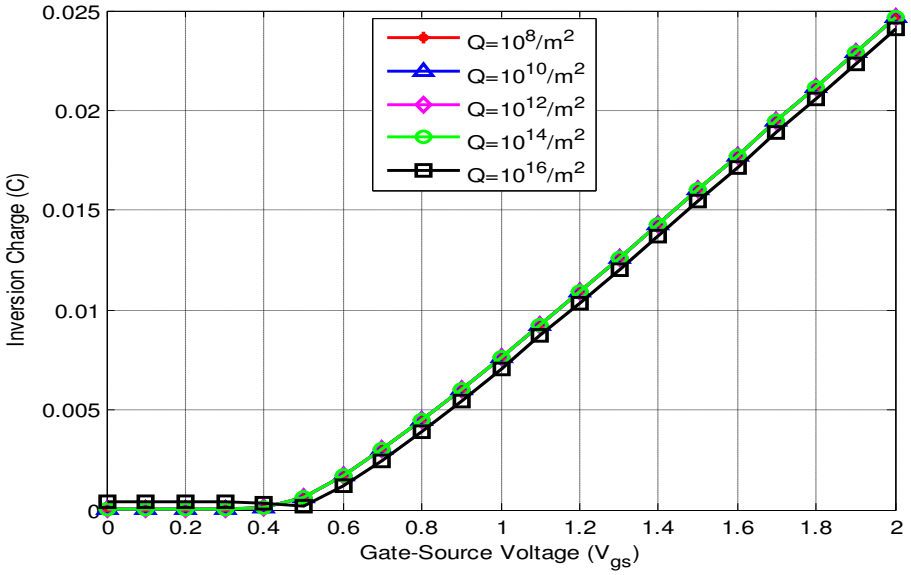


Fig. 3.12 The response of gate-to-source voltage (V_{gs}) over the inversion charge with different implantation doses.

Although, the doping level should be adjusted so that it does not degrade the mobility, and further the processing speed of the device. It is illustrated through the Fig. 3.12 that as the doping dose increases the threshold voltage of the device,

and hence would affect the off-state current of the device as the gate controllability on the channel increases.

3.5. Summary

The numerical modelling using Poisson's equations for un-doped and Gaussian doped silicon body of the surrounding gate MOSFET is performed. The analytical results of the device show that the electric potential and electron density varies in proportion with the gate voltage, and the minimum potential lies at the center of the silicon body due to the symmetric characteristics. In addition to this, the surface potential variation beyond the threshold voltage is independent of the silicon body thickness and can only be varied by the variation of work function. The analytical expressions of the small-signal parameters as a function of surface potential are also derived and the results express the physics of the surrounding gate MOSFET effectively. In addition to this, to achieve the desired threshold voltage, the doping can be implemented. In the analysis, we have carefully opted values of projected range and stagger factor so as to make the device effective for low power VLSI designing and analyzed the variation with different implanted dose. The results predict that for the accurate device performance the implanted dose can be taken $Q = 10^{16}/m^2$.

CHAPTER 4

PARAMETRIC ANALYSIS OF DOUBLE-GATE MOSFET AND SURROUNDING GATE MOSFET THROUGH EQUIVALENT CIRCUIT

4.1. Introduction

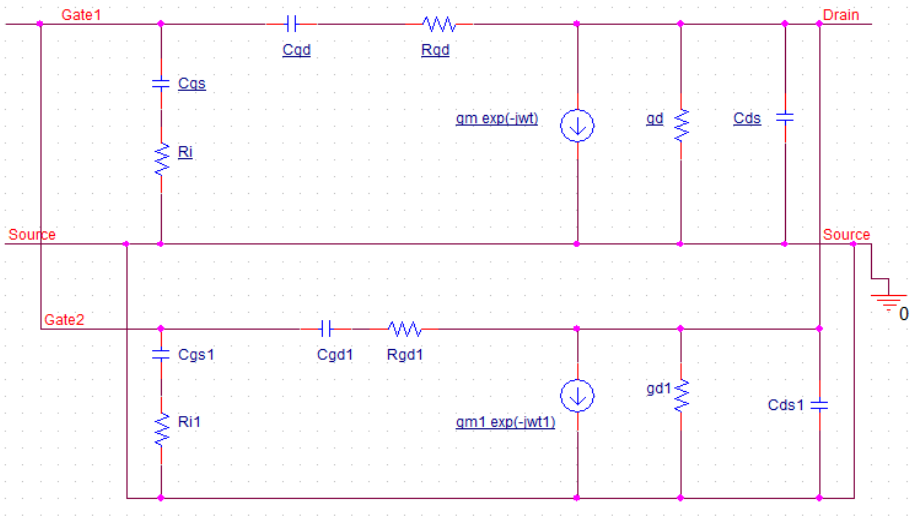
The communication market has been motivated by various forms of improvement in radio frequency integrated circuits. The demand of the industry is encouraging for the replacement of the costly, huge sized and more power consuming devices with low power and high density radio frequency devices. Moreover, the MOSFET are emerging as a better candidate for wireless communication and Radio frequency applications as the scaling of dimensions is being done to increase the speed of the device and further to improve the RF performance [168]. However, it is seen that, the MOSFET must be operated in the moderately inverted region so as to achieve the desired circuit performance in ultra low power RFIC design [62]. In addition to this, Lee and Cheng [63] also analyzed that the MOSFETs has much higher (Low frequency limit (LFLs) as compared with BJTs which is useful for RFIC design as well as generating HF distortion model for MOSFETs. Moreover, it is also seen that as the scaling approaches 50 nm range the unity gain frequency reaches to GHz regime which are very useful for high speed and high frequency application [169-170]. Although, a large signal model is needed to describe the device characteristics in the whole operating frequency regime, but for the analysis of the device at high frequency usually the S-parameters are used. This chapter presents the analysis based on the equivalent circuit approach, similar to the approach applied [171, 172], then the y-parameters are analytically calculated which further are used to extract the S-parameters. As the double-gate and surrounding-gate MOSFET can be scaled down to much smaller dimensions, which can further result in increase in packing density and reduced short channel effects (SCE). Therefore, analysis of both the device behaviour at the high range of frequency is the main point of interest. Although,

the ESD protection design should be applied to the RF and mm-wave circuits, which would further optimize the RF performance [173].

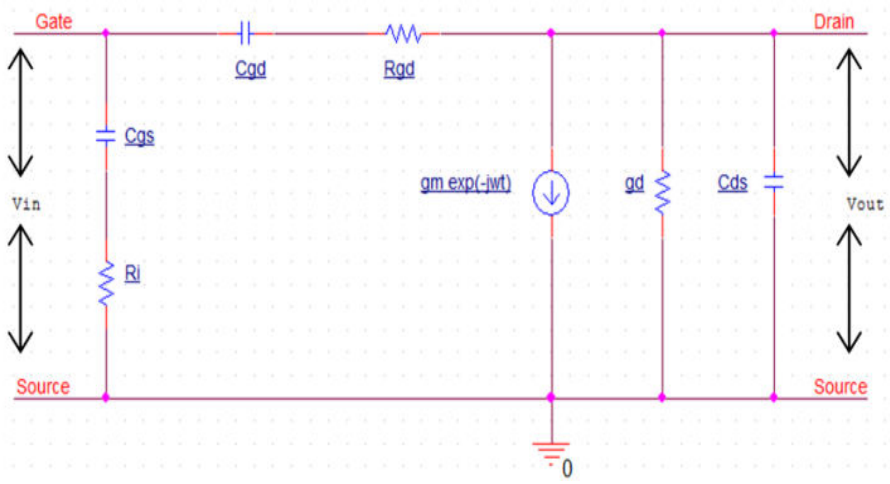
4.2. Model Formulation

4.2.1. Admittance Parameters

The small signal equivalent circuits in the form of two-port networks for Double gate MOSFET and Surrounding gate MOSFET are shown in Fig. 4.1 (a), (b) respectively, which are analyzed using the network analysis technique. The transient time t is defined as: $t = \frac{1}{2\pi f_t}$ and and f_t is the cutoff frequency depending upon the value of capacitances and trans-conductance $f_t = \frac{G_m}{2\pi(C_{gd}+C_{gs})}$. It is illustrated in Fig. 1(a) that, the DG MOSFET with same potential applied to both the gate is a combination of two parallel connected single gate MOSFET. Therefore, for the circuit analysis, the parallel connected two-port network analysis is performed. However, in Fig. 4.1(b) the single 1-port analysis is performed for the surrounding-gate MOSFET.



(a)



(b)

Fig. 4.1 The small signal equivalent circuit model for the (a) double-gate MOSFET, and (b) surrounding-gate MOSFET.

The equivalent circuits contain the intrinsic elements which can be derived for a particular gate-to-source voltage (V_{gs}) and drain-to-source voltage (V_{ds}). However, based on the network analysis technique the Y-parameters for both the devices can be derived. By using the Kirchhoff's current law for both the devices, the input port current and the output port current can be evaluated in terms of the intrinsic small signal parameters. Moreover, based on these current expressions the admittance parameters can be computed which are given in the form of the following expressions:

$$Y_{11} = \frac{I_1}{V_{gs}}\Big|_{V_{ds}=0} \tag{4.1}$$

$$Y_{12} = \frac{I_1}{V_{ds}}\Big|_{V_{gs}=0} \tag{4.2}$$

$$Y_{21} = \frac{I_2}{V_{gs}}\Big|_{V_{ds}=0} \tag{4.3}$$

$$Y_{22} = \frac{I_2}{V_{ds}}\Big|_{V_{gs}=0} \tag{4.4}$$

where, Y_{11} is the input admittance parameter, Y_{12} is the reverse transfer admittance, Y_{21} is forward transfer admittance and Y_{22} is the output admittance.

For the double-gate MOSFET the Y-parameters can be written as:

$$Y_{11} = 2\left(jwC_{gd} + \frac{jw\,C_{gs}}{1+w^2{C_{gs}}^2R_i} + \frac{w^2{C_{gs}}^2R_i}{1+w^2{C_{gs}}^2R_i}\right) \tag{4.5}$$

$$Y_{12} = 2\left(-jwC_{gd}\right) \tag{4.6}$$

$$Y_{21} = 2\left(\frac{g_m e^{-jwt}}{1+jw\,C_{gs}R_i} - jwC_{gd}\right) \tag{4.7}$$

$$Y_{22} = 2\left(jwC_{ds} + jwC_{gd} + g_d\right) \tag{4.8}$$

However, for surrounding-gate MOSFET Y-parameters are computed as:

$$Y_{11} = jwC_{gd} + \frac{jw\,C_{gs}}{1+w^2{C_{gs}}^2R_i} + \frac{w^2{C_{gs}}^2R_i}{1+w^2{C_{gs}}^2R_i} \tag{4.9}$$

$$Y_{12} = -jwC_{gd} \tag{4.10}$$

$$Y_{21} = \frac{g_m e^{-jwt}}{1+jw\,C_{gs}R_i} - jwC_{gd} \tag{4.11}$$

$$Y_{22} = jwC_{ds} + jwC_{gd} + g_d \tag{4.12}$$

4.2.2. Scattering parameters

It is seen that the parameters such as the open circuit impedance parameters (Z-parameters), short circuit admittance parameters (Y-parameters), hybrid parameters (H-parameters) cannot be accurately measured at high frequencies due to difficulty in obtaining perfect short/open circuit as the wire inductance and parasitic capacitance take over the measurements. In addition to this, the active devices may be unstable under open and short condition. Therefore, S-parameters are useful for the analysis in high frequencies as here the termination is provided by the characteristic impedance of either 50 Ω or 75 Ω. In addition to this, the waves used to define the parameter (incident and reflected waves), fully characterize the defined two-port network. Moreover, the S-parameters are important as they are used to determine the signal power gain and various other figures of merit [174].

In a two port network, the S-parameters can be defined by the following relationship between the scattering waves (incident wave, reflected wave).

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{4.13}$$

Where, a_1 is the incident wave on port 1, b_1 is the reflected wave from port 1 and a_2 is the incident wave on port 2 and b_2 is the reflected wave from port 2. In addition to this, S_{11} represents the input reflection coefficient, S_{12} is reverse transmission coefficient with input matched, S_{21} is the forward transmission coefficient and S_{22} is the output reflection coefficient. When combined, these parameters are known as scattering parameters.

However, the scattering parameters are computed by direct conversion from the previously calculated Y-parameters given as:

$$S_{11} = \frac{(1-Z_0Y_{11})(1+Z_0Y_{22})+(Z_0{}^2Y_{12}Y_{21})}{(1+Z_0Y_{11})(1+Z_0Y_{22})-Z_0{}^2Y_{12}Y_{21}} \tag{4.14}$$

$$S_{12} = \frac{-2Z_0Y_{11}}{(1+Z_0Y_{11})(1+Z_0Y_{22})-Z_0{}^2Y_{12}Y_{21}} \tag{4.15}$$

$$S_{21} = \frac{-2Z_0Y_{22}}{(1+Z_0Y_{11})(1+Z_0Y_{22})-Z_0{}^2Y_{12}Y_{21}} \tag{4.16}$$

$$S_{22} = \frac{(1+Z_0Y_{11})(1-Z_0Y_{22})+(Z_0{}^2Y_{12}Y_{21})}{(1+Z_0Y_{11})(1+Z_0Y_{22})-Z_0{}^2Y_{12}Y_{21}} \tag{4.17}$$

4.2.3. Gain Parameter Analysis for Amplifier Design

Several gains of the device such as unilateral power gain (U_T) and maximum stable power gain (G_{MS}) are discussed, which are useful when designing this device as amplified at the specified frequency regime of the spectrum [175]. The unilateral power gain is the maximum power gain that can be achieved when the two ports are simultaneously matched and there is no internal feedback.

$$U_T = \frac{\frac{\left|\frac{S_{21}}{S_{12}}-1\right|^2}{2}}{k\left|\frac{S_{21}}{S_{12}}\right|-Re\left[\frac{S_{21}}{S_{12}}\right]} \tag{4.18}$$

where, *k* is the stability factor

$$k = \frac{1-|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}S_{21}|} \tag{4.19}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{4.20}$$

The device is stable only when $k > 1$. Similarly, the maximum stable power gain is the gain that can be achieved by resistively loading the network, which can be achieved when the mismatch between the input and the output is reduced such that $k = 1$. The maximum value of the output port can be reduced.

$$G_{MS} = \frac{|S_{21}|}{|S_{12}|} \tag{4.21}$$

4.2.4. Capacitive model, operating as a switch

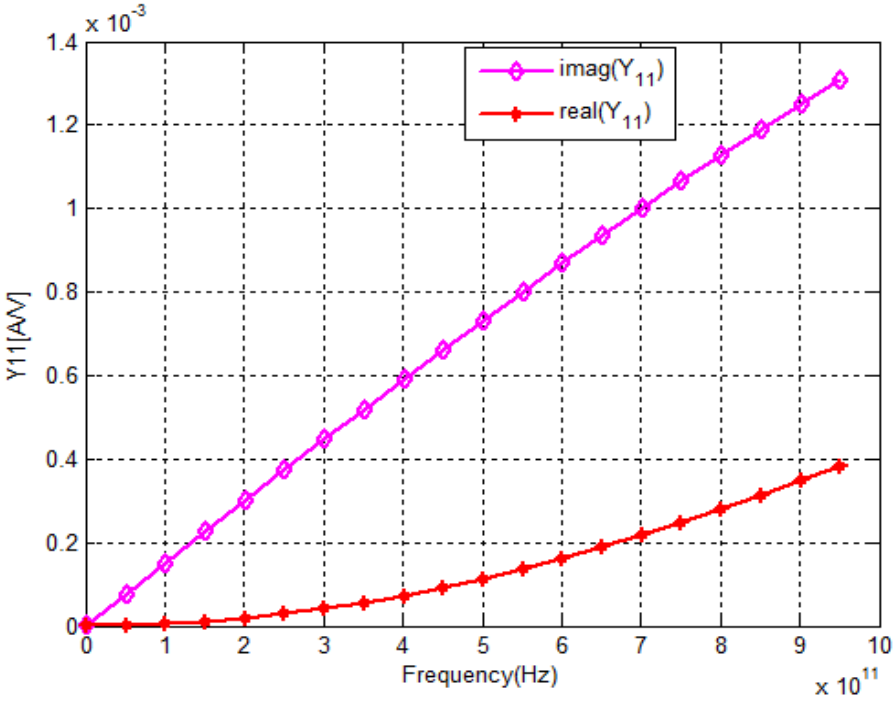
The MOSFET model, operating as a switch can be designed with the help of the different capacitances and resistances. However, the number of capacitances is different for both the device structures, i.e. surrounding-gate MOSFET has three types of capacitance and the double gate MOSFET has double capacitance compared to that of the surrounding-gate MOSFET. In the on-state, bulk related capacitances are not present, therefore less signals will be coupled to the substrate for both the devices i.e. double-gate MOSFET and surrounding-gate MOSFET. Moreover, lesser will be the dissipation into substrate resistance. However, when the transistors are in cut-off region, higher isolation can be provided by increasing the gate related and drain related capacitances

4.3. Simulation results

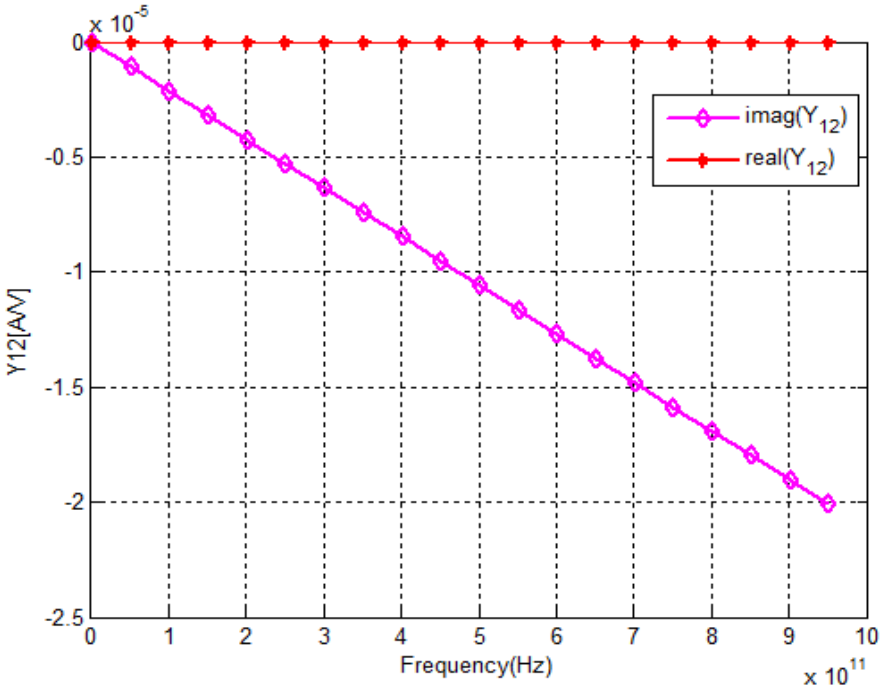
In this section, we have presented the simulation results of double-gate MOSFET and surrounding-gate MOSFET through the equivalent circuit approach.

4.3.1. Double-Gate MOSFET

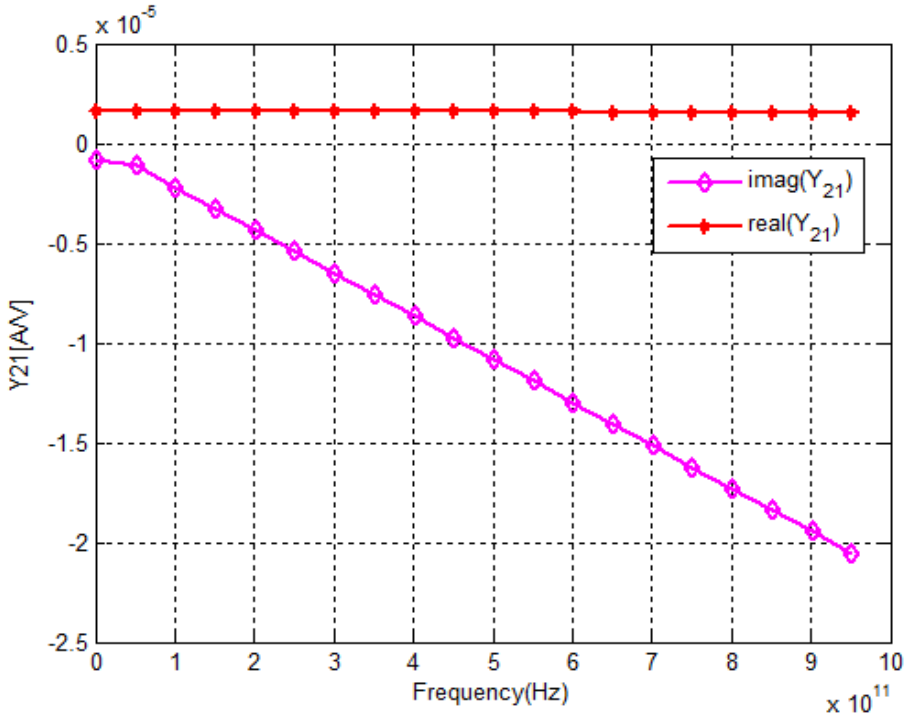
Fig. 4.2 shows the Y-parameter analysis of the DG MOSFET with t_{ox}= 2 nm, t_{si}= 40 nm and L_g= 1 µm and the biasing of the device is V_{gs}= 1 V and V_{ds}= 0.5 V.


x 10^-3
1.4
1.2
1
0.8
0.6
0.4
0.2
0
Y11[A/V]
imag(Y11)
real(Y11)
0
1
2
3
4
5
6
7
8
9
10
Frequency(Hz)
x 10^11

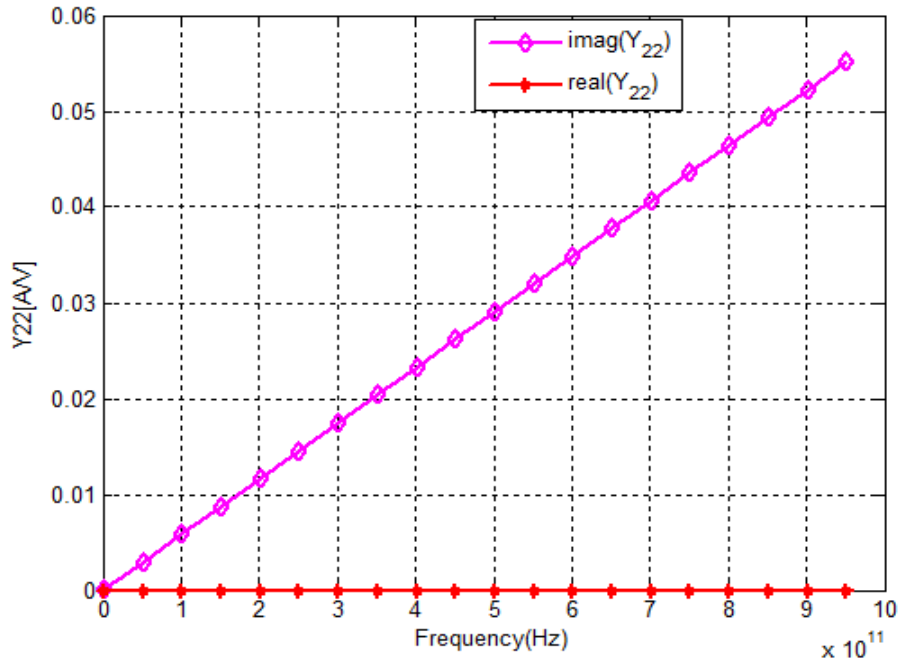
(a)


x 10^-5
0
-0.5
-1
-1.5
-2
-2.5
Y12[A/V]
imag(Y12)
real(Y12)
0
1
2
3
4
5
6
7
8
9
10
Frequency(Hz)
x 10^11

(b)

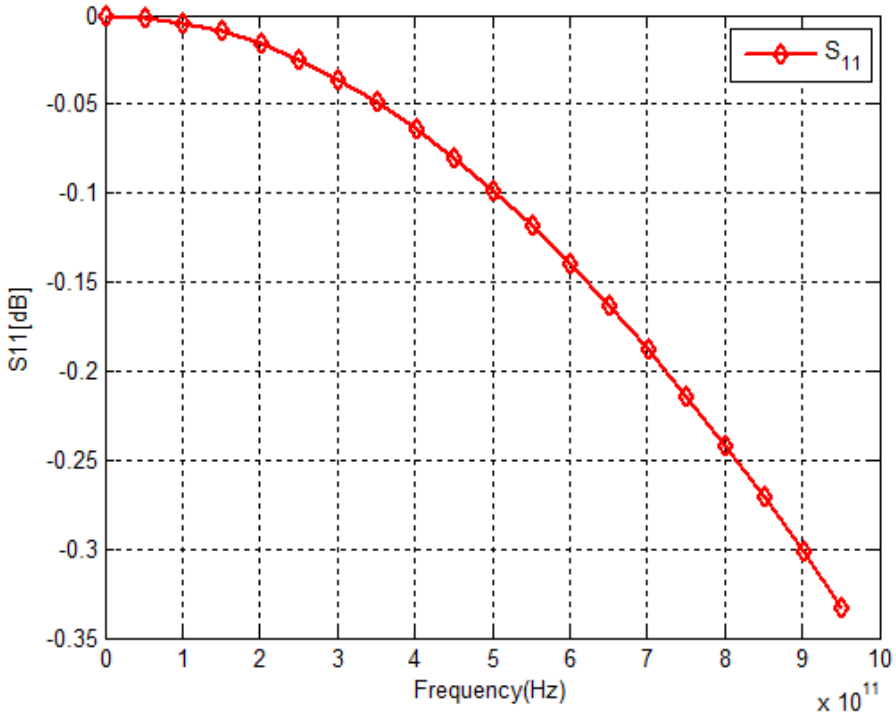


(c)

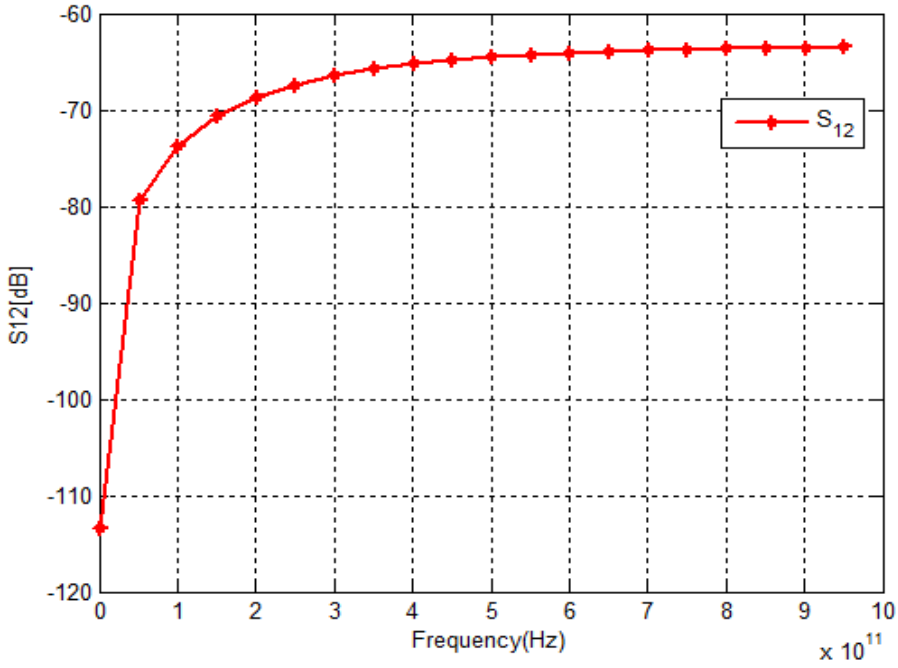


(d)

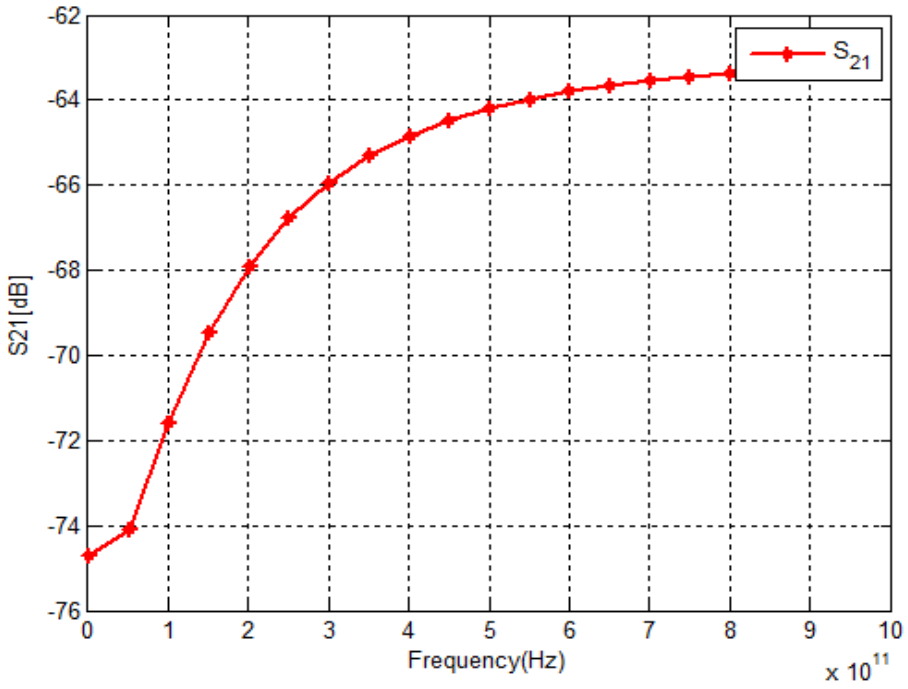
Fig. 4.2 Y-parameters for DG MOSFET (a) Y_{11}, (b) Y_{12}, (c) Y_{21}, and (d) Y_{22}.


S11
0
-0.05
-0.1
-0.15
-0.2
-0.25
-0.3
-0.35
S11[dB]
0
1
2
3
4
5
6
7
8
9
10
Frequency(Hz)
x 10^11

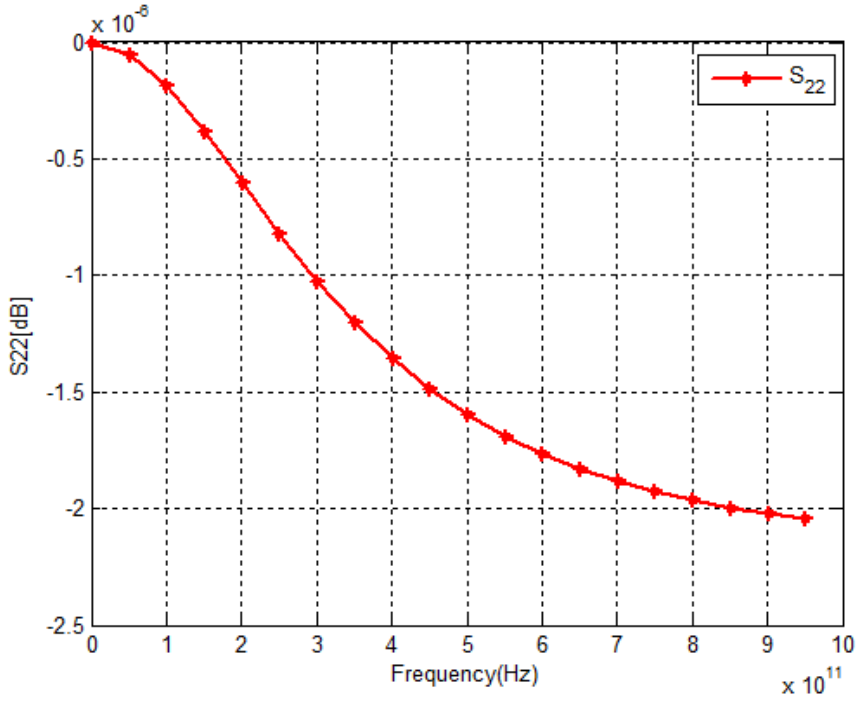
(a)


S12
-60
-70
-80
-90
-100
-110
-120
S12[dB]
0
1
2
3
4
5
6
7
8
9
10
Frequency(Hz)
x 10^11

(b)



(c)



(d)

Fig. 4.3 S-parameter analysis for DG MOSFET (a) S_{11}, (b) S_{12}, (c) S_{21}, and (d) S_{22}.

Fig. 4.3 shows the analyzed S-parameters calculated analytically using equivalent circuit of DG MOSFET with t_{ox}= 2 nm, W = 40 nm, L = 1 µm, V_{gs} = 1 V and V_{ds} = 0.9 V. S_{11} represents the input reflection coefficient and it is illustrated in the Figure 4.3(a) that the S_{11} is high and shows little variation with the frequency. S_{12} represents the reverse isolation parameter which is the leakage factor from the output port to the input port and Figure 4.3(b) suggests that high frequency this factor is significant due to the variation of the capacitances at high frequency. S_{21} represents the amount of power transferred from the input port to the output port and Figure 4.3(c) illustrates that as the frequency increases the parameter increases. S_{22} represents the output reflection coefficient and (d) shows that the parameter decreases with the frequency.

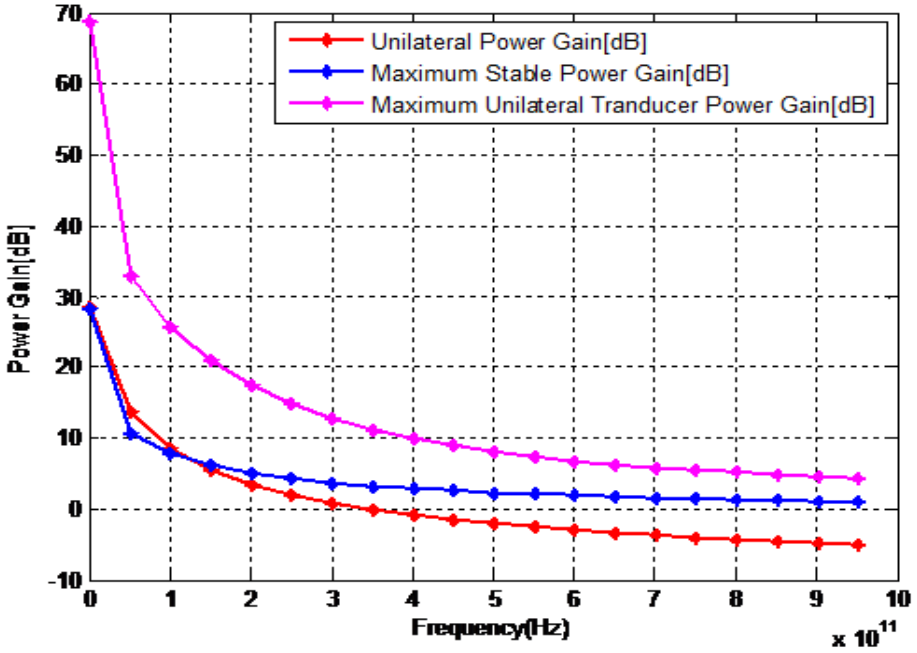
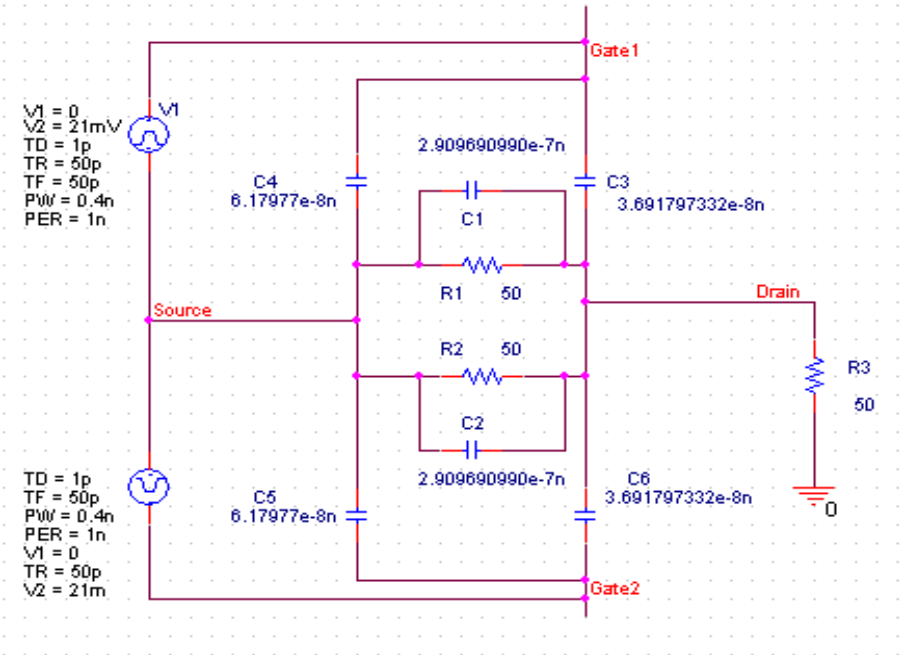


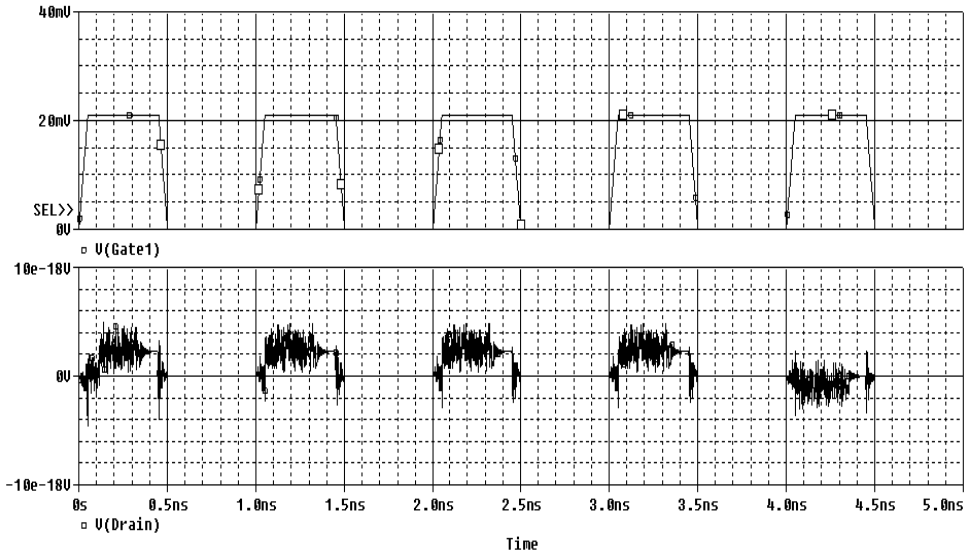
Fig. 4.4 The power gain analysis of DG MOSFET.

Fig. 4.4 represents the power gain achieved by the DG MOSFET over the range of frequencies. The unilateral power gain is the gain achieved when the input and the output port are matched simultaneously and the feedback as neutralized by adding a feedback network. As the frequency increase, this gain decreases exponentially and the decrease is less at high frequency due to the dual gate

controllability and by extrapolating the curve for the gain of 1 dB, the maximum frequency of oscillation can be inferred from the Fig. 4.4 to be around 254 GHz. The gain achieved when the two ports are simultaneously matched is known as maximum stable power gain and it is predicted by the Fig. 4.4 that as the frequency increases the input-output mismatch decreases. In addition to this, the gain always remains above 0 dB, which suggests the major figure-of-merit for low noise amplifiers. The maximum unilateral transducer power gain is the ratio of power delivered to load to the power available at the source when the neutralization is provided which further enhances the maximum power transfer. In addition to this, all these gains are constant with the frequency only due to the dual gate controllability as suggested by Fig. 4.4. Therefore, the DG MOSFET with the analyzed dimensions is useful for high frequency applications. However, it can be analyzed by the Fig. 4.4 that the highest amplifier gain achieved by the DG MOSFET is approximately 5 dB. Fig. 4.5 shows that by applying the input voltage of 21 mV, the pulse width of 0.4 ns and 50 ps and 1 ps rise/fall time and delay respectively, drain current only flows when voltage supply is ON. Therefore the switch has a clear cut-off status.



(a)



(b)

Fig. 4.5 Design of DG MOSFET with SPICE (a) capacitive model, operating as an on-state switch, and (b) input signal applied to gates and output signal applied at the drain.

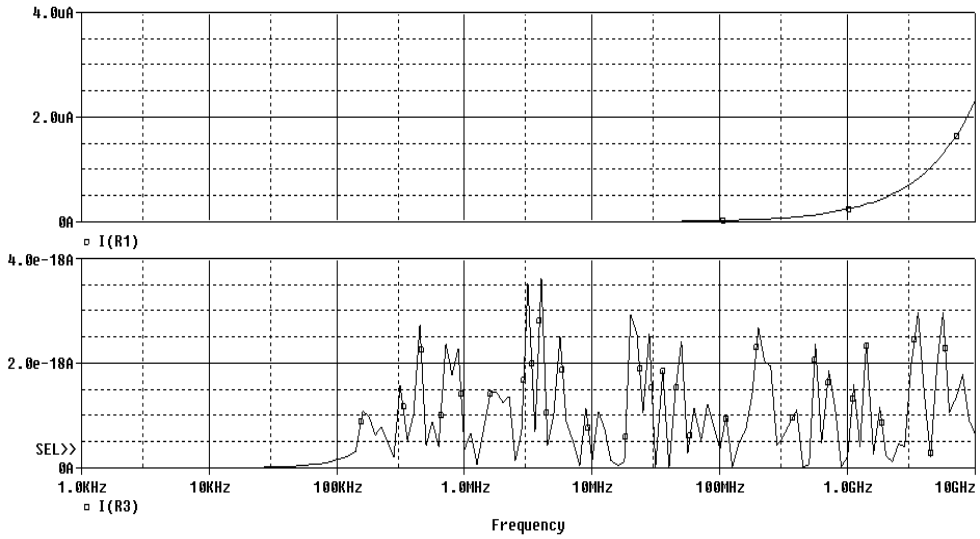
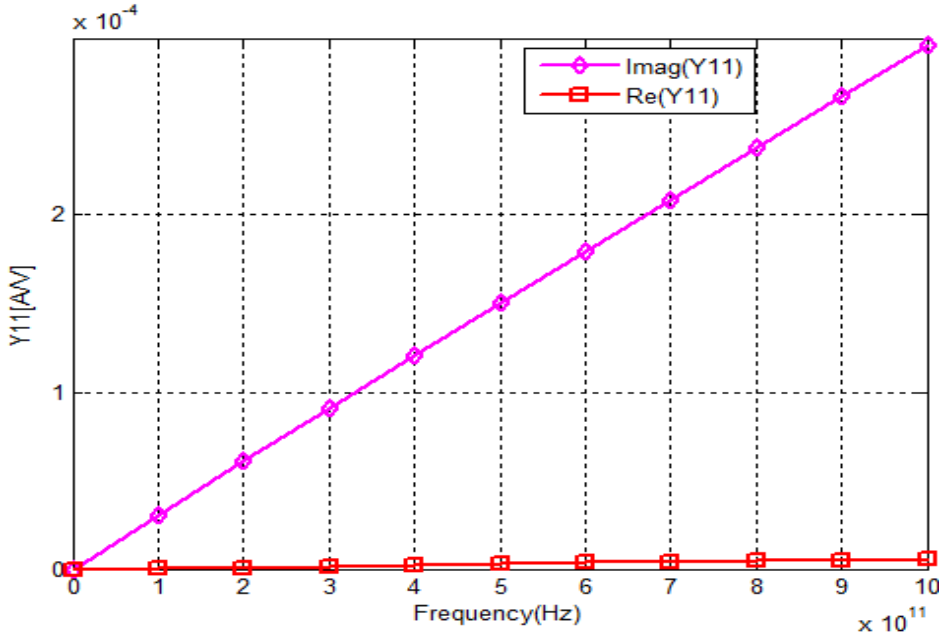


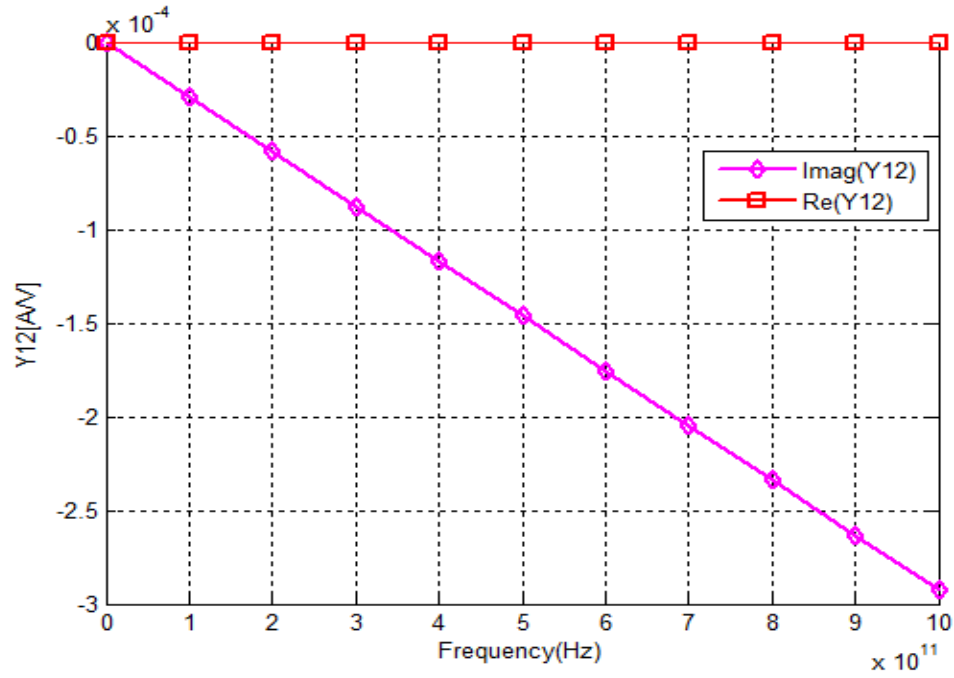
Fig. 4.6 The source current and drain current variation when the AC signal applied to the DG- gate MOSFET.

Fig. 4.6 shows the small drain current flows when the source current increases exponentially for the applied AC supply.

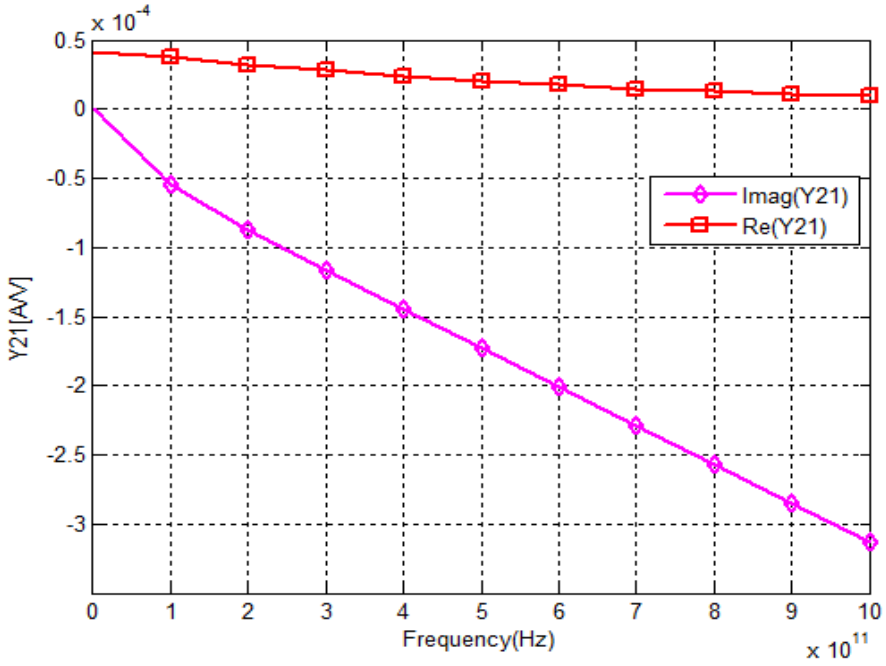
4.3.2. Surrounding-Gate MOSFET



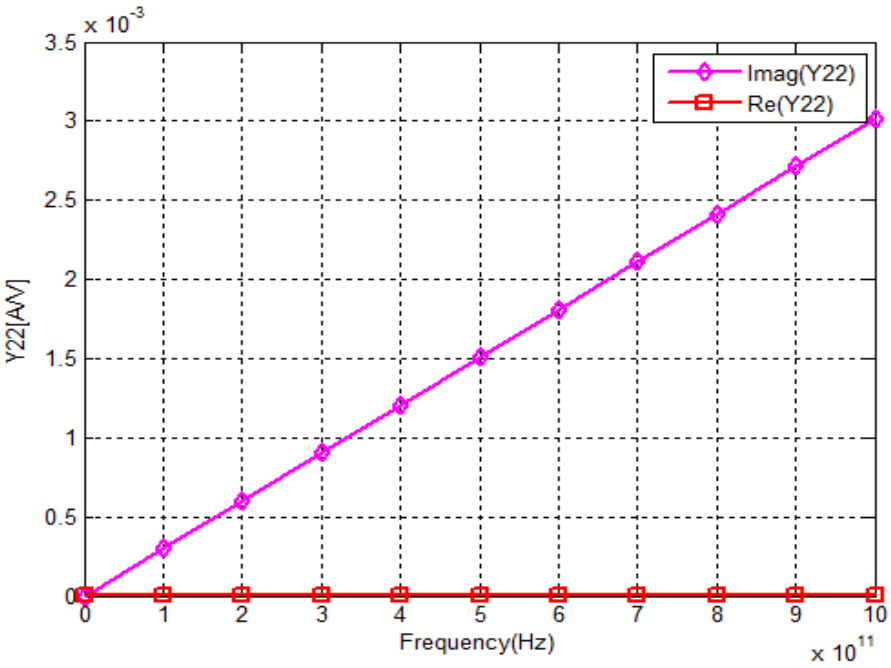
(a)



(b)



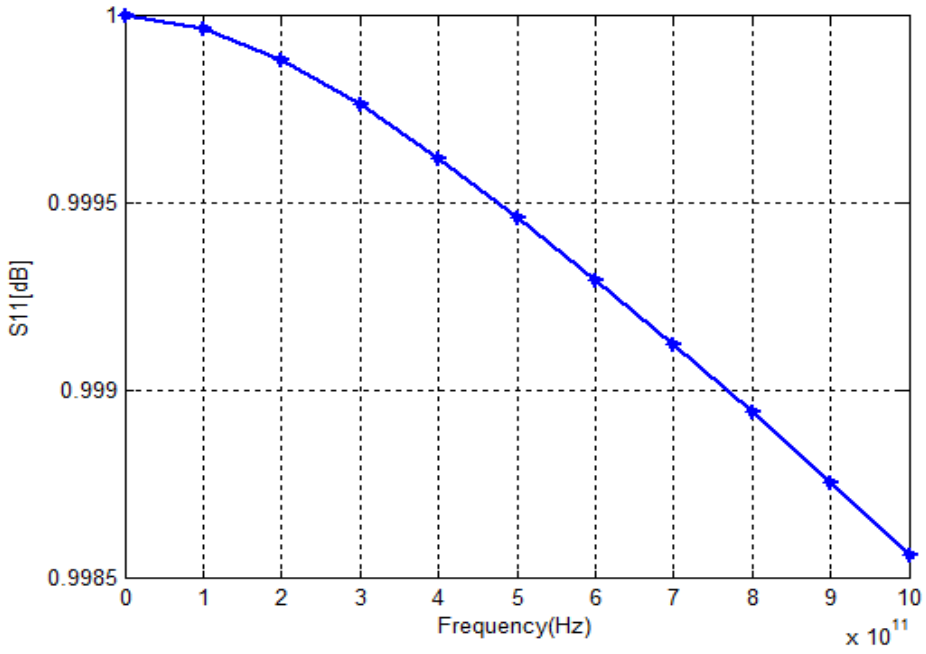
(c)



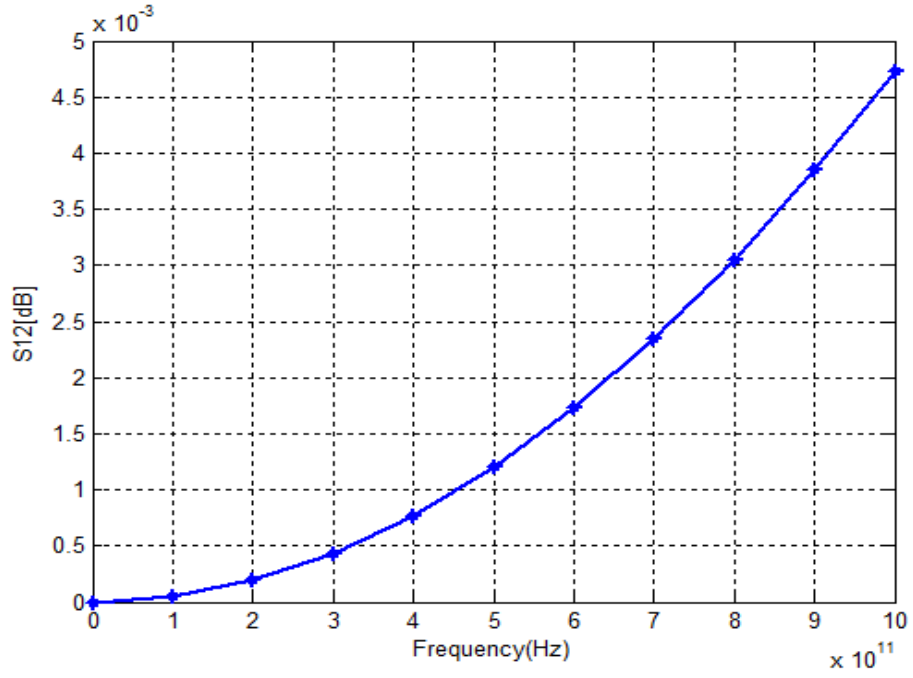
(d)

Fig. 4.7 Real and imaginary parts different Y-parameters of surrounding gate MOSFET (a) Y_{11}, (b) Y_{12}, (c) Y_2, and (d) Y_{22}.

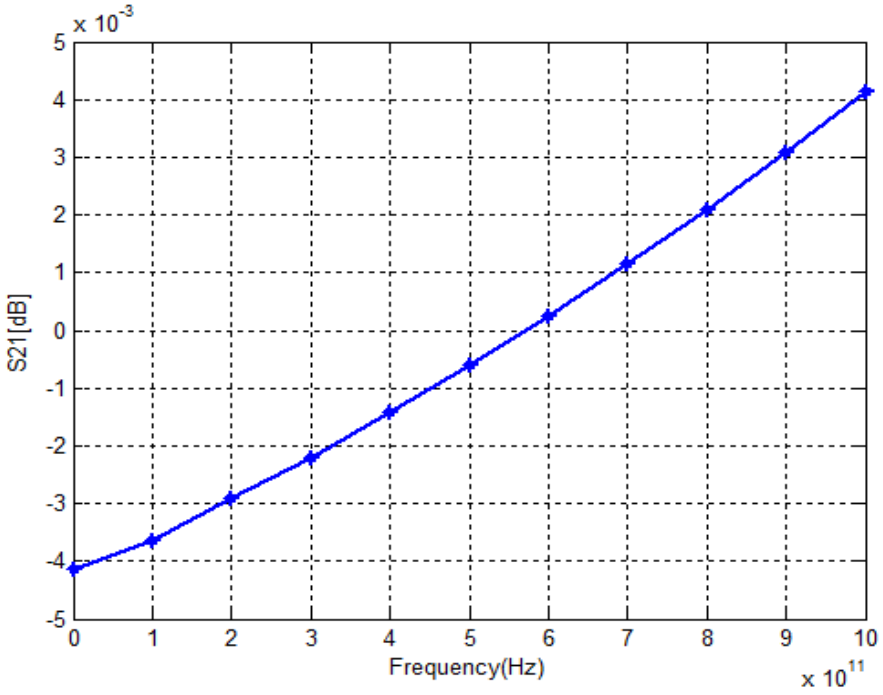
Fig. 4.7 shows the analyzed Y-parameters for the dimensions of t_{ox}= 2 nm, R= 20 nm and L_g= 90 nm, the biasing applied to the surrounding gate MOSFET is V_{gs}=1 V and V_{ds}=0.9 V.



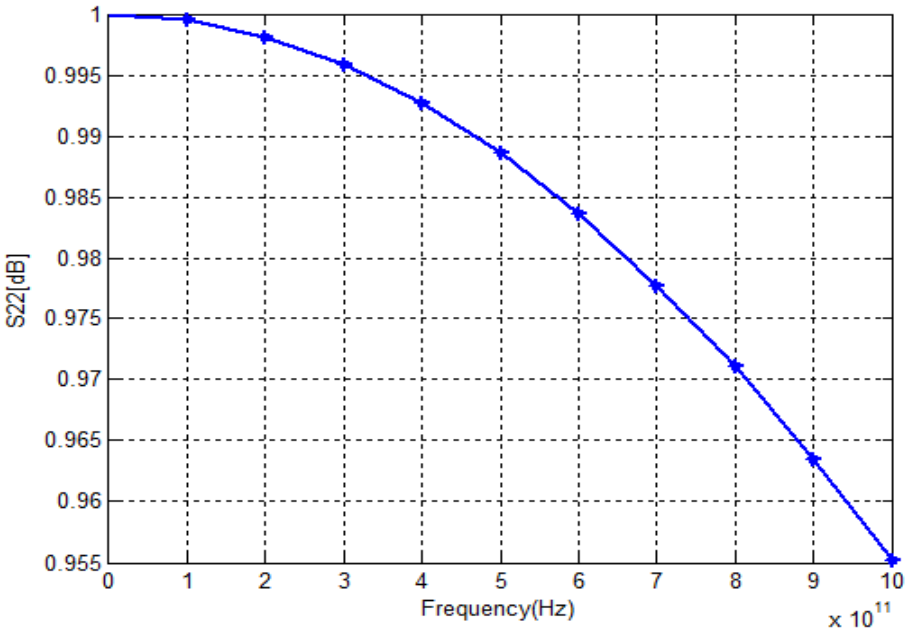
(a)



(b)



(c)



(d)

Fig. 4.8 S-parameter analysis of surrounding-gate MOSFET (a) S_{11}, (b) S_{12}, (c) S_{21}, and (d) S_{22}.

The frequency response of the s-parameters of the surrounding gate MOSFET are shown in Fig. 4.8. These parameters are computed analytically using the intrinsic equivalent circuit model with V_{gs} = 1V and V_{ds} = 0. 9 V with t_{ox} = 2 nm, R = 20 nm and L_g = 50 nm. Fig. 4.8(a) shows S_{11} is high and shows little variation with the frequency. Figure 4.8(b) suggests that high frequency S_{12} is significant due to the significant effect of the capacitances at high frequency. Figure 4.8 (c) illustrates that the maximum power transfer (S_{21}) from the input port to output port increases as the frequency increases. S_{22} represents the output reflection coefficient and Fig. 4.8(d) shows that the parameter decreases with the frequency. The power gain variation with frequency for V_{ds} = 0. 9 V and V_{gs} = 1 V of the surrounding gate MOSFET for the chosen dimension as shown in Fig. 4.9. The unilateral power gain is the highest gain that the active port can achieve and the maximum frequency of oscillation is obtained when this gain becomes unity (approximately at 900 GHz).

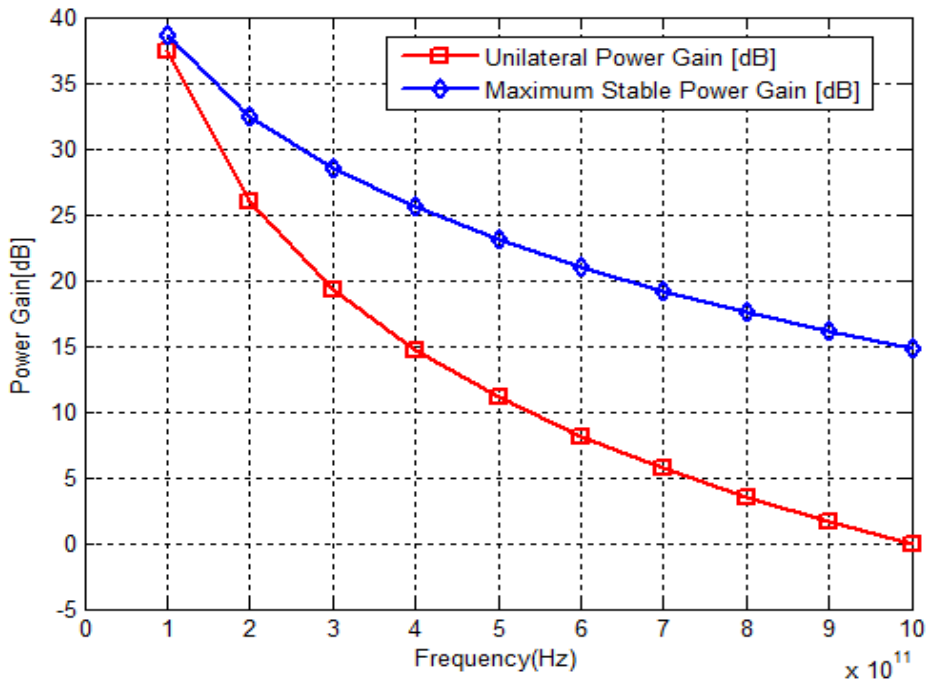
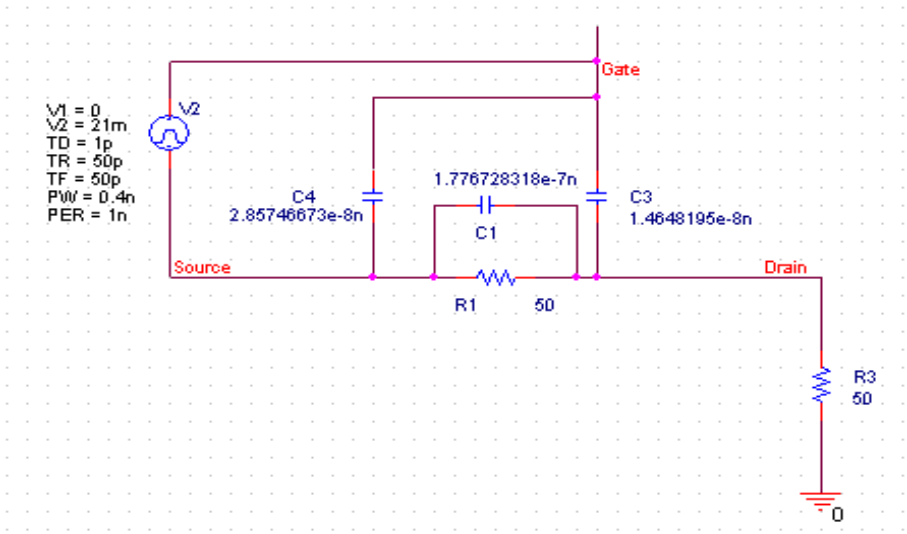


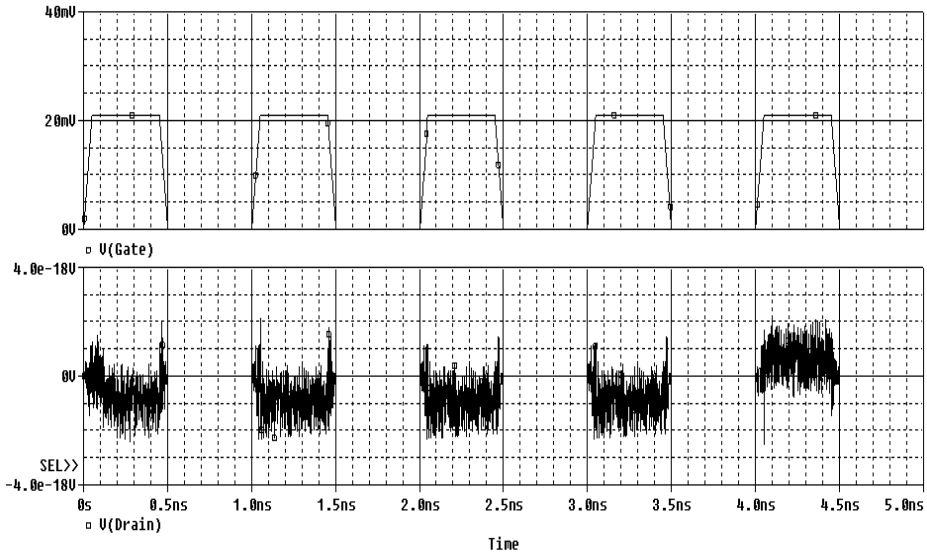
Fig. 4.9 The power gain of surrounding-gate MOSFET.

In addition to this, the maximum stable power gain is the maximum gain that can be obtained before the occurrence of instability. However, this gain decreases as

the frequency increases due to the decrease in mismatch between the input and output as shown Fig. 4.9.



(a)



(b)

Fig. 4.10 Design of the surrounding-gate MOSFET with SPICE (a) capacitive model, operating as an on-state switch, and (b) input signal applied to gates and output signal applied at drain.

Similar to the DG MOSFET Fig. 4.10 shows the excitation when the input signal changes from a low to high or vice versa. A clear cut-off status is also predicted through the Fig. 4.10.

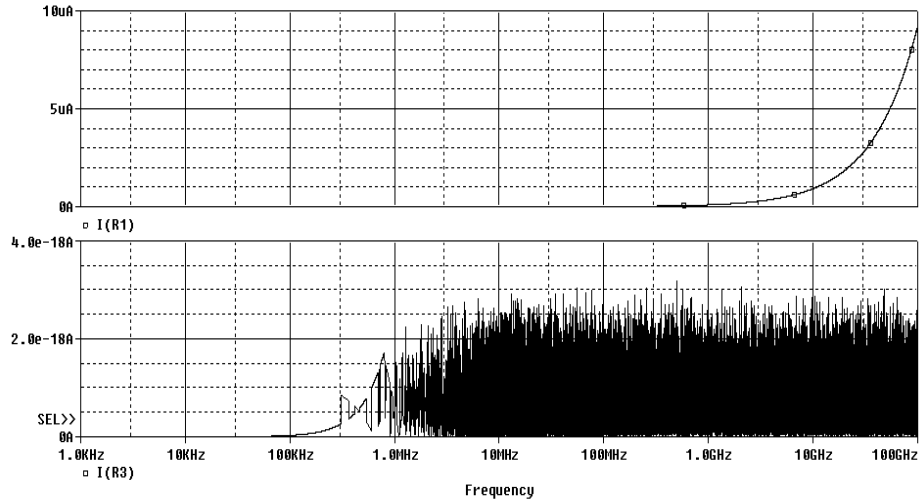


Fig. 4.11 Source current and drain current variation when AC signal applied to the surrounding-gate MOSFET.

Fig. 4.11 shows for capacitive model, the corresponding input and the output current variation with frequency. The input (source) current increases exponentially, with a small amount of output (drain) current flowing for that duration of time.

3.4. Summary

The chapter show the performance analysis of the DG MOSFET and surrounding-gate MOSFET for the analysis of device as a amplifier and as a switch based on the power gain analysis and on-state switch circuit analysis. It is analyzed that the surrounding gate MOSFET and double gate MOSFET have better device performance in term unilateral power gain and maximum stable power gain, which reveals that the circuit is significantly constructive in high frequency application. Moreover, the devices have good off-state characteristics.

Chapter-5

CONCLUSION AND FUTURE WORK

5.1. Conclusion

In this dissertation, the analytical modelling of symmetric DG MOSFET and surrounding-gate MOSFET with un-doped body is presented. The results reveal that both the devices with un-doped body show a significant volume inversion effect, which further increases the drain current below the threshold voltage. Moreover, the analytical expressions of the surface potential show that the threshold voltage is independent of the silicon body thickness. The continuity with a single set of mathematical expressions for both the devices is well predicted. Moreover, the intrinsic model for both the devices is purposed which are further characterized by the S-parameters and the power gain analysis. These parametric analyses revealed that the double gate MOSFET and surrounding-gate MOSFET are useful for high frequency applications with the higher achieved amplifier gain at the unity gain cut-off frequency for DG MOSFET and surrounding-gate MOSFET, respectively. However, the proper designing and optimization of the structure is required for the certain high frequency applications. Moreover, the surrounding gate MOSFET with Gaussian doping is also analyzed which prove to be an effective for achieving the desired threshold voltage in the nano-meter regime. By carefully opting for the values of the projected range and the stagger factor the surrounding gate MOSFET is useful for the applications need low power VLSI designing. Although, the accurate performance of the device can be maintained by opting the implantation dose of $10^{16}/m^2$, otherwise the mobility degradation would vary the device characteristics.

5.2. Future Scope

The dissertation discusses the analytical modelling of DG MOSFET and surrounding-gate MOSFET based on gradual channel approximation. Although,

the modelling can be extended further by including the horizontal electric field component in the channel, which would further able to include various SCE when device scaling approaches its scaling limit.

The analysis of the quantum mechanical effects would also be a wide research area when the thickness of the silicon body reaches to 5 nm. DG MOSFET and surrounding-gate MOSFET are promising for RF applications. The development of RFIC design using these two devices would also be interesting research areas.

Moreover, the model for Gaussian doped surrounding gate MOSFET can be extended further by developing the expressions for I-V and C-V characteristics. In addition to this, based on the intrinsic device parameters and optimization of the device structural parameters, the performance of Gaussian doped surrounding-gate MOSFET for high frequency application can also be analyzed.

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