JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATIONS-2022

B.Tech-V Semester (CS/IT)

COURSE CODE (CREDITS): 18B11CI514 (3) MAX. MARKS: 15

COURSE NAME: Computer Organization & Architecture

COURSE INSTRUCTORS: Dr. Vivek Sehgal, Dr. Pardeep Kumar, Sh. Praveen Modi, Dr. Vipul Sharma & Dr. Pankaj Dhiman. MAX. TIME: 1 Hour

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Note: *All questions are compulsory. Marks are indicated against each question in square brackets.*

Q1. An instruction is stored at location 3000 with its address field at location 3001. The address field has the value 4500. A processor register R1 contains the number 2000. Evaluate the effective address if the addressing mode of the instruction is **(i)** Direct **(ii)** Immediate **(iii)** Relative **(iv)** Register **(v)** Register Indirect **(vi)** Index with R1 as the index register.

[CO-2] [3]

Q2. Derive the mathematical expression for speed up that can be achieved using n processor system instead of a uniprocessor system. **[CO-2] [2]**

Q3. A compiler designer is trying to decide between two code sequences for a particular machine. Based on the hardware implementation, there are three different classes of instructions: Class A, Class B and Class C, and they require one, two and three cycles respectively.

The first code sequence has 5 instructions: 2 of A, 1 of B and 2 of C.

The second code sequence has 6 instructions: 4 of A, 1 of B and 1 of C.

Code Sequence	**Class A**	**Class B**	**Class C**
First	2	1	2
Second	4	1	1

a. Which code sequence will be faster?

b. What is the CPI of each sequence? **[CO-1] [2]**

[PTO]

Q4. A processor has 16 integer registers (R0, R1,… , R15) and 64 floating point registers (F0, F1,… , F63). It uses a 2 byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3, and Type 4. Type-1 category consists of four instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of fourteen instructions, each with one integer register operand and one floating point register operand (1R+1F). Type-4 category consists of N instructions, each with a floating point register operand (1F). Find the maximum value of N.

[CO-1] [3]

Q5. What is the difference between RISC and CISC? **[CO-1] [2]**

Q6.

a. Suppose there are "p" registers, each of size "q" bits, then how many multiplexers are used to design the bus? Also find out the size of each multiplexer. **[CO-1] [2]**

b. Given a memory element of size "4G x 10" bits. Find out the number of bits used to represent the address field. **[CO-2] [1]**