JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATIONS-2022

B.Tech-VII Semester (ECE)

COURSE CODE (CREDITS): 18B1WEC744 (3) MAX. MARKS: 15

COURSE NAME: FPGA BASED INTRUMENTATION SYSTEM DESIGN

COURSE INSTRUCTORS: ANUJ KUMAR MAURYA MAX. TIME: 1 Hour

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***Note:*** *All questions are compulsory. Marks are indicated against each question in square brackets.*

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Q1. What are the advantages of FPGA over ASIC? Explain in detail when and why FPGA implementation is preferred? [CO1] [3]

Q2. Implement the following logics using PAL and PROM with minimum possible connections: [CO2] [3]

$$F_1(A, B, C) = \sum m(1, 3, 4, 5)$$

$$F_2(A, B, C) = \sum m(0, 1, 2, 6, 7)$$

Q3. Discuss the FPGA architecture. What are the different programming technologies for reconfigurable FPGAs? [CO1] [3]

Q4. How any module is created and instantiated in Verilog? Design a 4 bit full adder using Gate level modeling. [CO2, CO5] [3]

Q5. What are different logic gates used in Verilog and how they are written? Discuss all the gates and its syntax in Verilog. [CO1] [3]