ZIGBEE BASED ELECTRONIC NOTICE BOARD

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By

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May’ 2016

DECLARATION BY THE SCHOLAR

I hereby declare that the work reported in the B-Tech thesis entitled**"Wireless Notice Board Using Zigbee"** submitted at**Jaypee University of Information Technology,Waknaghat,**is an authentic record of my work carried out under the supervision of**Mrs.VanitaRana**. I have not submitted this work elsewhere for any other degree or diploma.

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Date ( )

SUPERVISOR'S CERTIFICATE

This to certify that project report entitled "**Wireless Notice Board using Zigbee"**, submitted by**AnanditaGarg(123004)** and **SumehaMahajan(121106)** in partial fulfillment for the award of degree of Bachelor of Technology in Electronics and Communication Engineering to Jaypee University of Information Technology, Waknaghat, Solan has been carried out under my supervision. This work has not been submitted partially or fully to any other University or Institute for the award of this or any other degree or diploma to the best of my knowledge and belief.

Mrs.VanitaRana

Assistant Professor

Date:

ACKOWLEDGEMENT

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(SumehaMahajan) (AnanditaGarg)

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LIST OF ABBREVATIONS

AES	Advanced Encryption Standard
AMR	Automatic Meter Reading
CMOS	Complementary metal-oxide semiconductor
CPU	Central Processing Unit
EEPROM	Electrically Erasable Programmable Read-Only Memory
GSM	General Packet Radio Service
GPRS	General Packet Radio Service
IIL	Pulled Low Will Source Current
IE	Interrupt Enable
LCD	Liquid-crystal-display
LED	Light-emitting diode
PAN	Personal Area Network
PAS	Public Addressing System
MAC	Media Access Control
RF	Radio Frequency
RAM	Random Access Memory
TTL	Transistor Transistor Logic
WDT	Watch Dog Timer
WPAN	Wireless Personal Area Networks

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Abstract

This Project deals about designing a wireless notice board which can be accessed remotely using advanced Zigbee technology. Zigbee is a Personal Area Network technology based on the IEEE 802.15.4 standard. This technology is a low data rate, low power consumption, low cost wireless networking protocol targeted towards automation and remote control applications. In terms of battery life, cost, complexity of protocol stack and number of nodes participating in mesh network Zigbee is better than other WPANs, such as Bluetooth.

It is one of the new technologies in the embedded field to make the communication between microcontroller and computer. Zigbee uses a basic master –slave configuration suited to static star networks of many in frequently used devices that talk via small data packets. The hardware of the project consists of two parts :Zigbee transmitting module and Zigbee receiving module. The keyboard is connected n the transmitter side, whatever the text is typed on the transmitter side the same is received on the the receiver side. At any time the user can add or remove or alter the text according to his requirement.

The project is built around the AT89S51 microcontroller from Atmel. The microcontroller provides all the functionality of the display and wireless control. Assembly language is used to program the microcontroller.

CHAPTER1

INTRODUCTION

1.1 Objective

Wireless technology has been making tremendous progress over the past few years. The ever increasing use of wireless networks serves as an indicator of the progress in the area of wireless networks. The demand for wireless technology is increasing not only in industrial applications but also for domestic purposes.

The **Zigbee** based alphanumeric display system is a essential device in any organization or public utility place like bus and railway stations. The main aim of this project is to design an SMS driven automatic display which reduces the manual operation. The information can in turn be updated instantly at the desired location. This project deals about an advanced hi-tech wireless notice board.

1.2 Zigbee Technology

Zigbeeis a IEEE 802.15.4-based specification for a suite of high-level communication protocols used to create personal area networks with small, low-power digital radios.

The technology defined by the ZigBee specification is intended to be simpler and less expensive than other wireless personal area networks (WPANs), such as Bluetooth or Wi-Fi. Its low power consumption limits transmission distances to 10–100 meters line-of-sight, depending on power output and environmental characteristics. ZigBee devices can transmit data over long distances. ZigBee is typically used in low data rate applications that require long battery life and secure networking. ZigBee has a defined rate of 250 kbit/s, best suited for intermittent data transmissions from a sensor or input devices. ZigBee is a low-cost, low-power,wireless mesh network standard targeted at wide development of long battery life devices in wireless control and monitoring.applications. Zigbee devices have low latency, which further reduces average current.

The main advantages of ZigBee are:

- Power saving, as a result of the short working period, low power consumption of communication, and standby mode
- Reliability: Collision avoidance is adopted, with a special time slot allocated for those communications that need fixed bandwidth so that competition and conflict are avoided when transmitting data. The MAC layer adopts completely confirmed data transmission, that is, every data packet sent must wait for the confirmation from the receiver
- Low cost of the modules, and the ZigBee protocol is patent fee free
- Short time delay, typically 30 ms for device searching, 15 ms for standby to activation, and 15 ms for channel access of active devices
- Large network capacity: One ZigBee network contains one master device and maximum 254 slave devices. There can be as many as 100 ZigBee networks within one area

- Safety: ZigBee provides a data integrity check and authentication function. AES-128 is adopted and at the same time each application can flexibly determine its safety property.

The main disadvantages of ZigBee include short range, low complexity, and low data speed. Due to their high cost, GSM and GPRS are normally used in concentrators to transmit data to the main station, or in high end multi-function meters. ZigBee is used mainly in the concentrators, data collectors, repeaters, and meters installed in the urban distribution AMRsystems and prepayment systems. Because of the good real time capability of RF, meters are often equipped with a remote control function.

1.3 Comparison of other technologies

FEATURES	**IEEE 802.11**	**BLUETOOTH**	**ZIGBEE**
Battery Life	Hours	Days	Years
Complexity	Very complex	Complex	Simple
Nodes	32	7	64000
Latency	Upto 3seconds	10 Seconds	30 milliseconds
Range	100m-1000m	10m	10-75m
Data rate	11Mbps	1Mbps	250 Kbps

Table 1.1: Comparison of other technology

CHAPTER 2

LITERATURE SURVEY

2.1 Previous Work

Public Addressing System (PAS) is an electronic sound and amplification distribution system with a microphone, amplifier and loudspeakers. PA systems are widely used to make announcements in public, institutional and commercial buildings and locations. In PA systems cost, quality and expansion are the major factors that affect the working and implementation of the system. The Zigbee based monitoring and controlling help us to improve the quality and performance, reduce cost, power and complexity and simplifies expansion.

Several projects have been undertaken subjected to wireless controlling, delivering and monitoring system for a public addressing system by combining embedded and Zigbee wireless network technology for low power and low cost data communication in fields where wired communication is expensive and complex.

Most of the existing systems have complex designs due to excessive wiring and are difficult to expand in order to meet the necessities of the customer. The Blue Tooth based PA systems suffers from noisy air, distance and line of sight communication.

Embedded systems changed the nature of consumer electronics, home appliances, automobile, office automation, business equipments and security systems. An embedded system is nearly any computing system other than a desktop, laptop, or mainframe computer. Computing systems are embedded within large electronic or consumer devices Wireless based automation is a prime concern in our daily life.

A number of the cost effective and energy saving systems developed using Zigbee networks. The systems used in smart energy, medical and home automation which has mesh topology can be developed effectively using Zigbee.

2.2 Applications

ZigBee applications are varied and the flexibility of the stack includes the option to include Manufacturer Specific Protocols. However, key application profiles are:

Smart Metering – The smart metering profile has been developed with features such as metering support, demand response and load control support, pricing support, text message support and security.

Home Automation – The Home Automation profile is the first application space where multiple products from multiple vendors are truly interoperable allowing users to mix and match products to enhance their digital lifestyle. Lighting control, thermostats, occupancy and motion sensors, security systems, door and window sensors, as well as fixed and mobile keypads all occupy the ZigBee home automation space and can be bound together to make sophisticated home automation behaviours.

CHAPTER3

FUNDAMENTAL CONCEPTS

3.1 Transmission Module

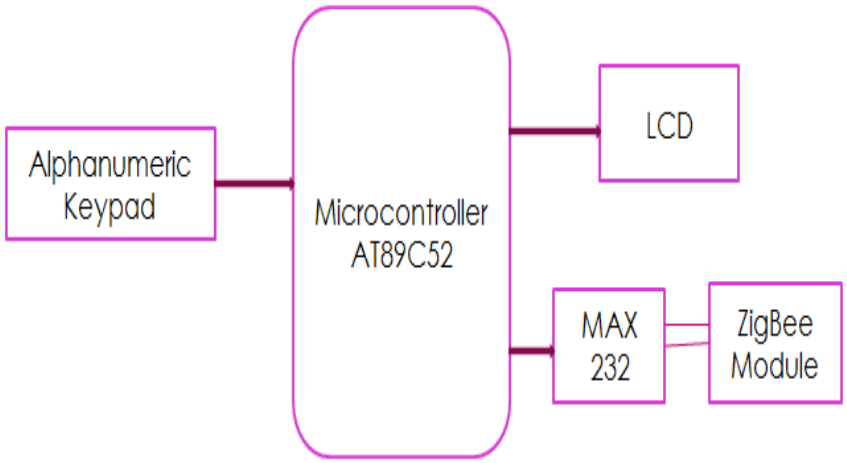


Figure 3.1: Block diagram of transmitter

3.2 Reception Module

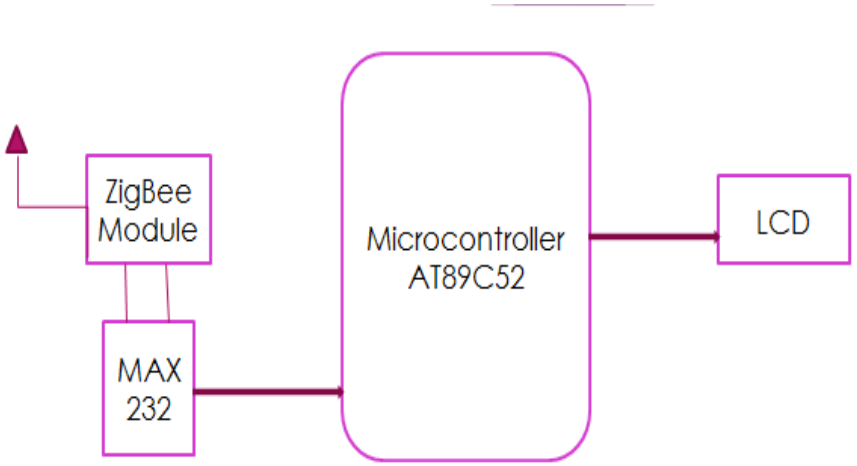


Figure 3.2: Block diagram of receiver

Our proposed model consists of two modules i.e. one Transmitter and one Receiver module. The transmitter module consists of Alphanumeric Keypad through which the person at the transmitter end types the message to be displayed on the notice board. The message is fed to the microcontroller which is then transmitted wirelessly via MAX232 which will convert the signals compatible with the TTL logic circuits with maximum input voltage of 3.3 V to the Zigbee module.

The receiver module placed at the remote end consists of Zigbeemodule interfaced with a microcontroller via MAX 232 for displaying messages on LCD for the mass display.

CHAPTER 4

HARDWARE DESCRIPTION

4.1 AT89S51 Microcontroller

The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of In-System Programmable Flash memory. The device is manufactured using Atmel's high-density non-volatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional non-volatile memory programmer. By combining a versatile 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications. The AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

The 8051 microcontroller architecture

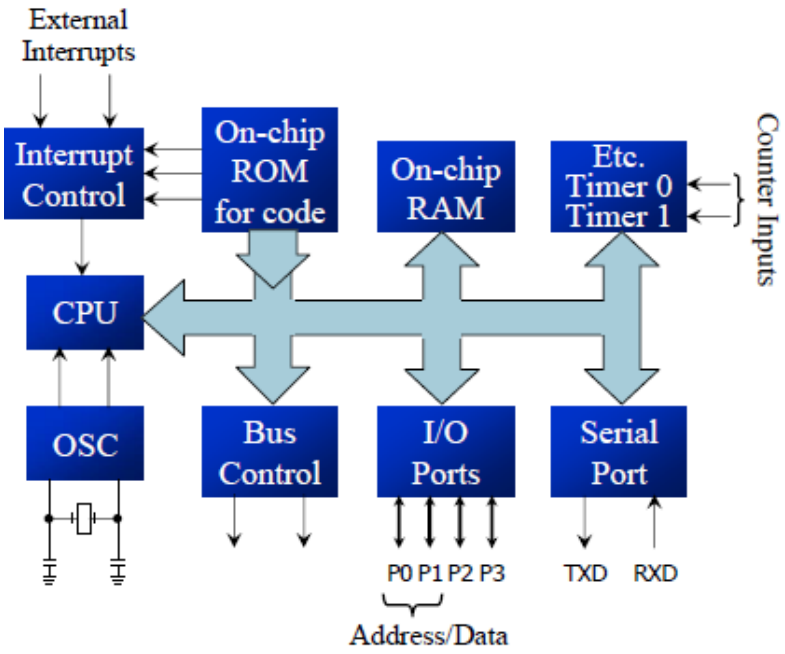


Figure4.1 : 8051microcontroller architecture

Figure shows the main features and components that the designer can interact with. You can notice that 89S51 has four different ports, each having eight input/output lines providing a total of 32 I/O lines. Those parts can be used to output data and other necessary information i.e. read and write to the LCD.

Most of the ports of 89S51 have dual function that means they can be used for two different functions- one is to perform I/O operations and second is to implement special features of the microcontroller like counting external pulses, interrupting the the program according to external events, performing serial data transfer or connecting the chip to the computer to update the software.

AT89S51 Pin Configuration

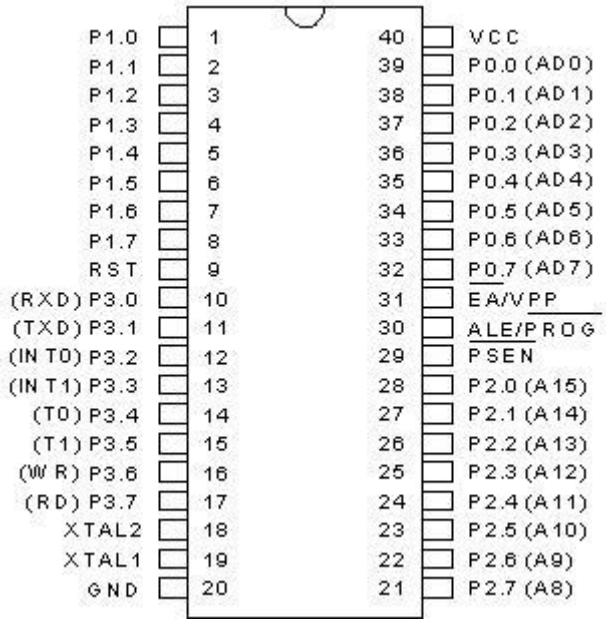


Figure 4.2: AT89S51 Pin Configuration

Pin Configuration Description

VCC - Supply voltage

GND - Ground

Port 0 - Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance i/p.Port 0 can also be configured to be the multiplexed low-order address/data bus during access to external program and data memory. In this mode, P0 has internal pull-ups. Port 0 also receivesthe code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1 -Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they

are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally beingpulled low will source current (IIL) because of the internal pull-ups. Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2- Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses ,Port 2 emits the contents of the P2 Special Function Register.

Port 3 -Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers cansink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the interPort Pin Alternate Functions P1.5 MOSI (used for In-System Programming) P1.6 MISO(used for In-System Programming) P1.7 SCK (used for In-System Programming) 5 2487D-MICRO–6/08 AT89S51 internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pull-ups. Port 3 receives some control signals for Flash programming and verification. Port 3 also serves the functions.

RST -Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/PROG- Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program

pulse input (PROG) during Flash programming. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set,

ALE- is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly put high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN - Program Store Enable (PSEN) is the read strobe to external program memory. When the AT89S51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP-External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however,that if lock bit 1 is programmed, EA will be internally latched on reset.

XTAL1-Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2-Output from the inverting oscillator amplifier

Registers and Memory

Special Function Register

A map of the on-chip memory area called the Special Function Register (SFR) . Not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Interrupt Registers

The individual interrupt enable bit are in IE register. Two priorities can be set for each of the five interrupt sources in IP register.

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory

If the EA pin is connected to GND, all program fetches are directed to external memory. On the AT89S51, if EA is connected to VCC, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles.To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Powerdown mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode. To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode. Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a

timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode. With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51.The 8051 has two timers,they can be used either as timers to generate a time delay. Both Timer 0 and Timer 1 are 16 bitswideSince 8051 has an 8-bit architecture, each 16-bits timer is accessed as two separate
registers of low byte and high byte.

Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts (INT0 and INT1), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 10-1. Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once. Note that Table shows that bit positions IE.6 and IE.5 are unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products. The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA=0,no interrupt is acknowledged. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
-	IE.6	Reserved
-	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit

Table4.1 : Functions of Interrupts

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset. Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an

enabled external interrupt (INT0 or INT1). Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before VCC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

4.216*2 LCD

16×2 LCD is used as output by the controller to show any data or any information to user .The name 16×2 LCD means 16 number of data can be can be written on two lines. The data can be numbers(0-9) or letters(A-Z) of any symbol like "$" ,"#".To show a number or alphabet on LCD screen we need to just send the ASCII value to the data pin. LCD module is a very common type of LCD module that is used in 8051 based embedded projects. It consists of 16 rows and 2 columns of 5×7 or 5×8 LCD dot matrices. It is available in a 16 pin package with back light ,contrast adjustment function and each dot matrix has 5×8 dot resolution.

4.2.1 Pin Description

VEE: Pin is meant for adjusting the contrast of the LCD display and the contrast can be adjusted by varying the voltage at this pin.

RS : High logic at the RS pin will select the data register and Low logic at the RS pin will select the command register. If we make the RS pin high and the put a data in the 8 bit data line (DB0 to DB7) , the LCD module will recognize it as a data to be displayed .

R/W : pin is meant for selecting between read and write modes. High level at this pin enables read mode and low level at this pin enables write mode.

E : pin is for enabling the module. A high to low transition at this pin will enable the module.

DB0 to DB7 :are the data pins. The data to be displayed and the command instructions are placed on these pins.

LED+ : is the anode of the back light LED and this pin must be connected to Vcc

LED-: is the cathode of the back light LED and this pin must be connected to ground.

PIN NO.	SYMBOL	DESCRIPTION	FUNCTION
1	Vss	Ground	0v
2	Vcc	Power supply for logic circuit	+5v
3	Vee	Lcd Contrast Adjustment	
4	RS	Instruction/Data Register Selection	RS=0 :Instruction Register
5	R/W	Read /Write Selection	R/W=0: Register Write
6	E	Enable Selection	
7	DB0	Data Input/Output Lines	8 bit: DB0-DB7
8	DB1		
9	DB2		
10	DB3		
11	DB4		
12	DB5		
13	DB6		
14	DB7		
15	LED+	SUPPLY VOLTAGE FOR LED+	+5V
16	LED-	SUPPLY VOLTAGE FOR LED-	0V

Table 4.2: Functions of LCD

+5V is provided to Vdd(pin2) and ground is provided to Vss(pin1) to provide power to LCD and its controller. Vee is used to control the contrast of the LCD .If ground is connected directly to this pin the contrast will be so low that the each pixel would get so dark that nothing could be read. If Vcc(+5V) is directly provided to it the contrast will be so high that the pixel wouldn't glow at all. So connect a resistance to ground in series with the pin.Twoimportant registers are present in the LCD.

One is data register and other is instruction command code register. If data is sent at data register the data is considered as data to be displayed on the LCD. If data is sent at instruction command code register the data is considered as command from user like to clear the screen or blink the cursor,etc.To let the LCD know whether the data on data line is command or a databyte to be displayed, RS is used.

->If **RS=0** the instruction code command register is selected and the data on data line is a command.

->If **RS=1** the data register is selected and the data on data line is to be displayed on screen.

LCD MODULE COMMANDS

16×2 LCD module has a set of preset command instructions. Each command will make the module to do a particular task. The commonly used commands and their function are given in the table below.

Code(hex)	Command to LCD Instruction Register
1	Clear display screen
2	Return home
4	Decrement cursor(shift cursor to left)
5	Shift display right
6	Increment cursor(shift cursor to right)
7	Shift display left
8	Display off, cursor off
A	Display off, cursor on
C	Display on, cursor off
E	Display on, cursor blinking
F	Display on, cursor blinking
10	Shift position cursor to left
14	Shift cursor position to right
18	Shift the entire display to left
1C	Shift the entire display to right
80	Force cursor to beginning to 1st line
C0	Force cursor to beginning to 2st line
38	2 lines and 5x7 matrix

Table 4.3: Commands of LCD

4.2.2 Interfacing with Microcontroller

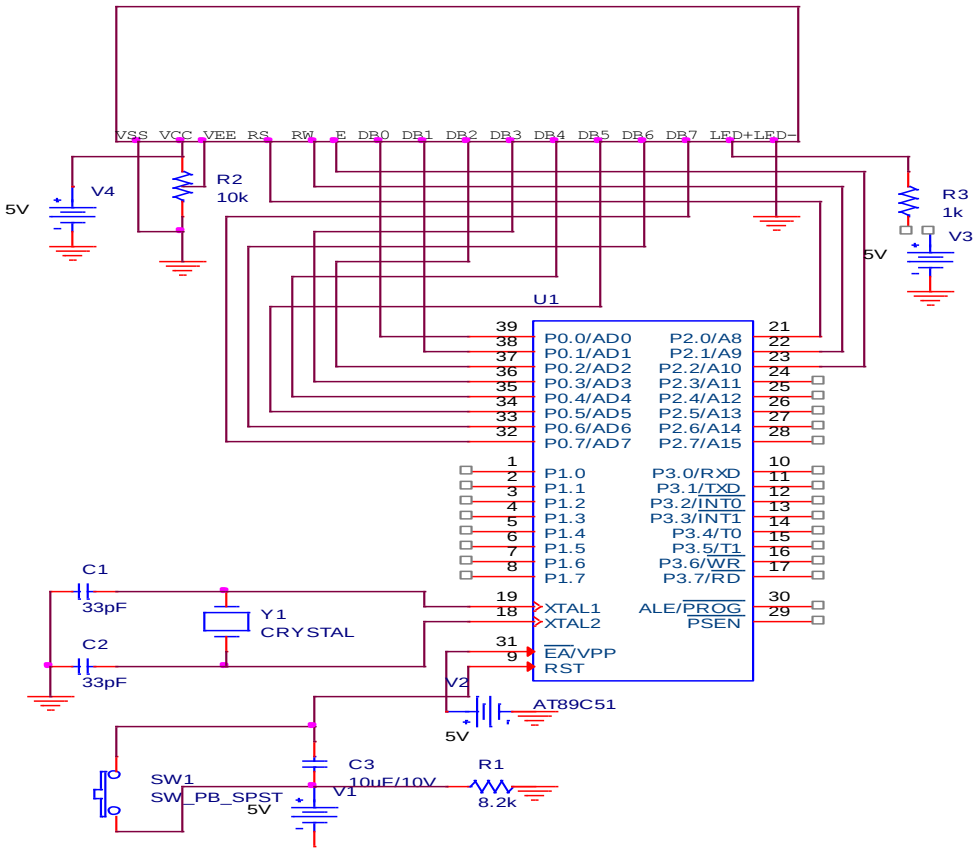


Figure 4.3: Interfacing with Microcontroller

The circuit diagram given above shows how to interface a 16×2 LCD module with AT89S1 microcontroller. Capacitor C3, resistor R3 and push button switch S1 forms the reset circuitry. Ceramic capacitors C1,C2 and crystal X1 is related to the clock circuitry which produces the system clock frequency. P1.0 to P1.7 pins of the microcontroller is connected to the DB0 to DB7 pins of the module respectively and through this route the data goes to the LCD module. P2.2, P2.1 and P2.0 are connected to the E, R/W, RS pins of the microcontroller and through this route the control signals are transffered to the LCD module. Resistor R1 limits the current through the back light LED and so do the back light intensity. POT R2 is used for adjusting the contrast of the display.

LCD initialization

The steps that has to be done for initializing the LCD display is given below and these steps are common for almost all applications.

- Send 38H to the 8 bit data line for initialization
- Send 0FH for making LCD ON, cursor ON and cursor blinking ON.
- Send 06H for incrementing cursor position.
- Send 01H for clearing the display and return the cursor.

Sending data to the LCD

The steps for sending data to the LCD module is given below. I have already said that the LCD module has pins namely RS, R/W and E. It is the logic state of these pins that make the module to determine whether a given data input is a command or data to be displayed.

- Make R/W low.
- Make RS=0 if data byte is a command and make RS=1 if the data byte is a data to be displayed.
- Place data byte on the data register.
- Pulse E from high to low.
- Repeat above steps for sending another data.

4.3 4x4 MATRIX KEYBOARD

A keypad is the most widely used devices of digital circuits, microcontrollers or telephone circuits. Many applications require large number of keys connected to a computing system. Provided that it for the most part holds numbers then it can additionally be known as a numeric keypad. In order to use it efficiently, we need a basic understanding of them. A matrix keypad consists of arrangement of switches in matrix format in rows and columns with the microcontroller I/O pins connected to the rows and columns of the matrix such that switches in each row are connected to one pin

and switches in each column are connected to another pin. A keypad is generally a matrix arrangement of tact switches which are basically push button switches.

Typically one port pin is required to read a digital input into the controller. When there are a lot of digital input that has to be read, it is not feasible to allocate one pin for each of them. This is when a matrix keypad arrangement is used to reduce the pin count.

Initially all switches are assumed to be released. So there is no connection between the rows and columns. When any one of the switches are pressed, the corresponding rows and columns are connected (short circuited). This will drive that column pin (initially high) low. Using this logic, the button press can be detected.

Here are the steps involved in determining the key that was pressed.

Step 1:

The first step involved in interfacing the matrix keypad is to write all logic 0's to the rows and all logic 1's to the columns.

Step 2:

Now the software has to scan the pins connected to columns of the keypad. If it detects a logic 0 in any one of the columns, then a key press was made in that column. This is because the event of the switch press shorts the C2 line with R2. Hence C2 is driven low.

Step 3:

Once the column corresponding to the key pressed is located, the next thing that the software has to do is to start writing logic 1's to the rows sequentially (one after the other) and check if C2 become high. The logic is that if a button in that row was pressed, then the value written to that row will be reflected in determined column (C2) as they are short circuited.

Step 4:

The procedure is followed till C2 goes high with logic high is written to a row. In this case, a logic high to the second row will be reflected in the second column.We already know the key press happened at column 2. Now we have detected that the key is in row 2. So, the position of the key in the matrix is (2,2).Once this is detected, its up to us to name it or provide it with a task in the event of the key press.

4.3.1 Interfacing with Microcontroller

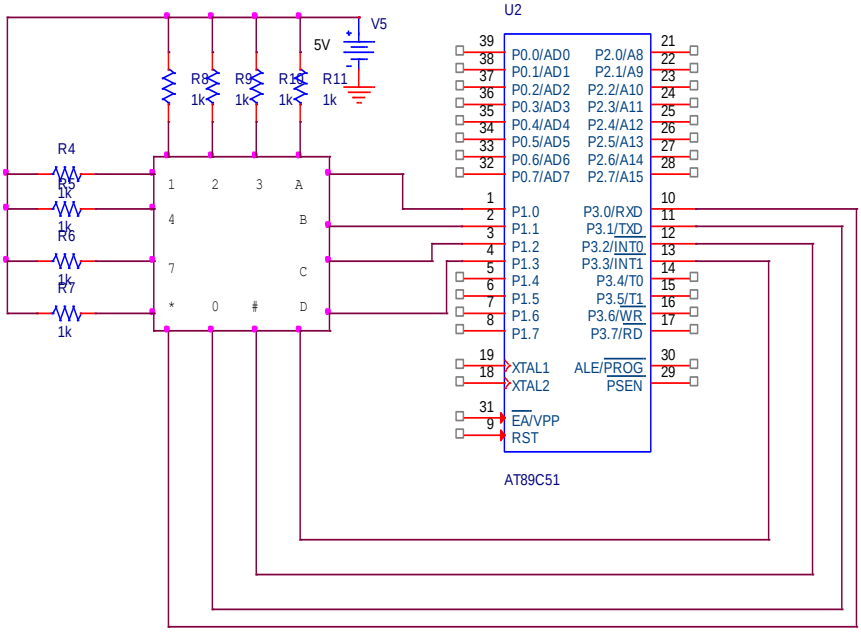


Figure 4.4:Interfacing with Microcontroller

10KΩ resistor and 10µF will provide the required Power On Reset (POR) signal to the 8051 microcontroller. 12MHz crystal is used to provide required clock for the microcontroller and 33pF capacitors will stabilize the oscillations of the crystal. AT89C51 can works upto 24MHz. We can choose the required frequency by changing the crystal and clock frequency in the project settings of Keil C. Keypad is connected to the Port P1 and column inputs pins are pulled up internally. 16×2 LCDis connected to Port P2 and P0. P0.0 and P0.1 pins are pulled up externally using 10KΩ resistors since Port P0 has no internal pull up.

4.4 MAX232

The **MAX232** is an integrated circuit first created in 1987 by Maxim Integrated Products that converts signals from a RS-232 serial port to signals suitable for use in TTL-compatible digital logic circuits. The MAX232 is a dual driver/receiver and typically converts the RX, TX, CTS and RTS signals.

The drivers provide RS-232 voltage level outputs (about ±7.5 volts) from a single 5-volt supply by on-chip charge pumps and external capacitors. This makes it useful for implementing RS-232 in devices that otherwise do not need any other voltages.

The receivers reduce RS-232 inputs, which may be as high as ±25 volts, to standard 5-volt TTL levels.

4.4.1 Pin Configuration and Description

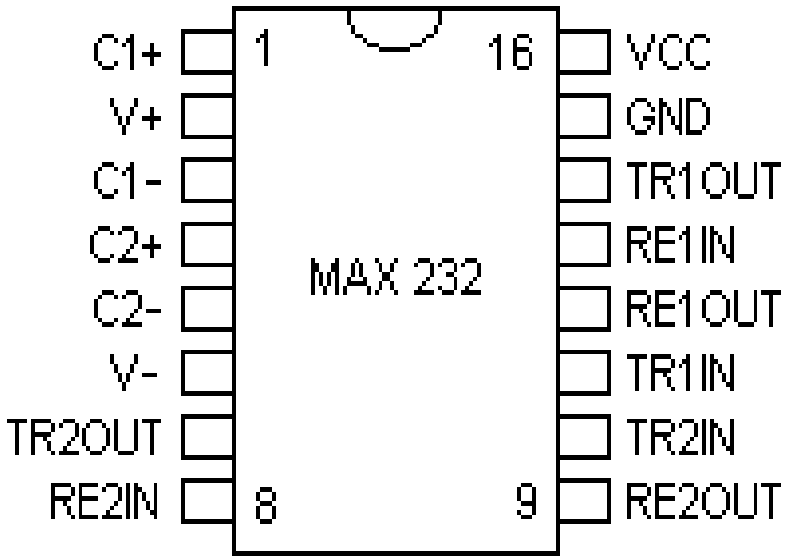


Figure 4.5: Pin Configuration and Description

PIN FUNCTIONS

Pin No	Pin Name	Description
1	C1+	Positive lead of C1 capacitor
2	VS+	Positive charge pump output for storage capacitor only
3	C1-	Negative lead of C1 capacitor
4	C2+	Positive lead of C2 capacitor
5	C2-	Negative lead of C2 capacitor
6	VS-	Negative charge pump output for storage capacitor only
7,14	T1OUT,T2OUT	RS232 line data output
8,13	R1IN,R2IN	RS232 line data input
9,12	R1OUT,R2OUT	Logic data output (to UART)
10,11	T1IN,T2IN	Logic data input (from UART)
15	GND	Ground
16	Vcc	Supply Voltage, Connect to external 5V power supply

Table 4.4: Pin Functions

4.4.2MAX232 Interfacing with Microcontroller

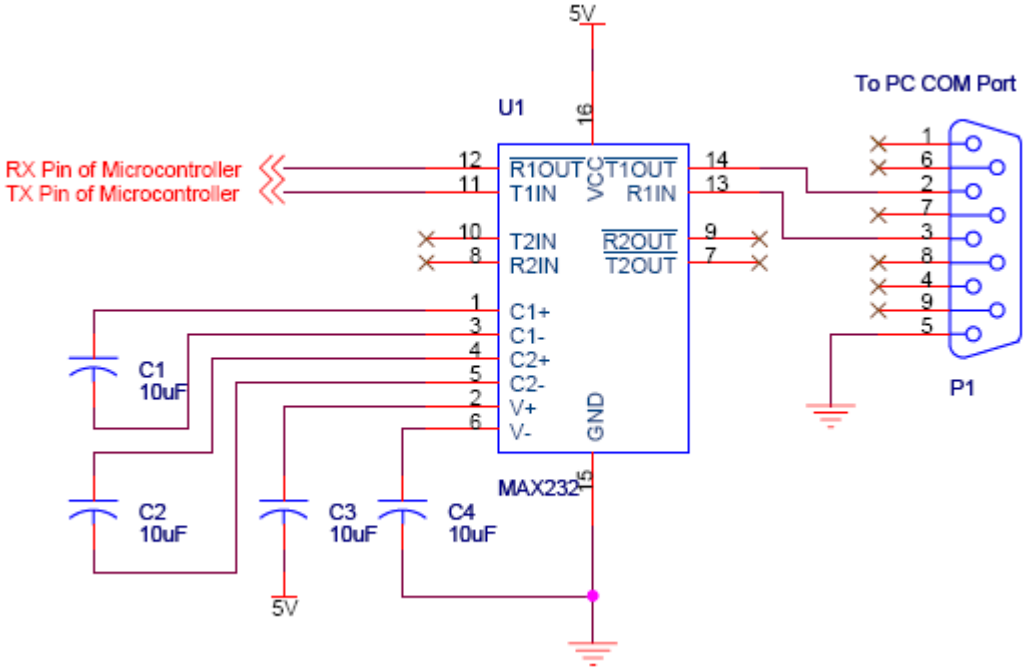


Figure 4.6: MAX232 Interfacing with Microcontroller

The circuit diagram consists of:

1. RS232
2. MAX232
3. AT89S51/52

RS232

DB-9 RS-232 is a serial I/O standard, used commonly in PCs and other devices. RS-232 (Recommended Standard 232) is a standard for serial binary data signals connecting between a DTE (Data terminal equipment) and a DCE (Data Circuit-terminating Equipment).

VOLTAGE LEVELS

The RS-232 standard defines the voltage levels that correspond to logical one and logical zero levels. Valid signals are plus or minus 3 to 25 volts. The range near zero volts is not a valid RS-232 level; logic one is defined as a negative voltage, the signal condition is called marking, and has the functional significance of OFF. Logic zero is positive, the signal condition is spacing, and has the function ON. So a Logic Zero represented as +3V to +25V and Logic One represented as -3V to -25V.

RS-232 LEVEL CONVERTERS

Usually all the digital ICs works on TTL or CMOS voltage levels which cannot be used to communicate over RS-232 protocol. So a voltage or level converter is needed which can convert TTL to RS232 and RS232 to TTL voltage levels. The most commonly used RS-232 level converter is MAX232. This IC includes charge pump which can generate

RS232 voltage levels (-10V and +10V) from 5V power supply. It also includes two receiver and two transmitters and is capable of full-duplex UART/USART communication.

PIN DIAGRAM

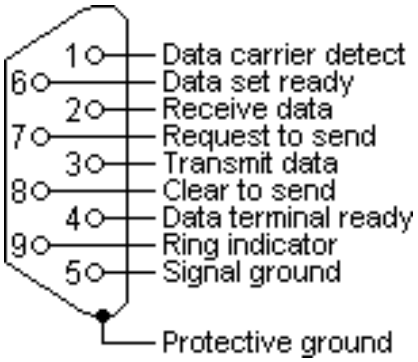


Figure 4.7: DB9

MAX232

The output of RS232 is not compatible with the TTL. Inorder to connect RS232 to AT89S51/52 microcontroller a converter is required. Here we make use of MAX232. This can convert the output of the microcontroller to the RS232 output level and vice versa. Usually, MAX232 consists of two line drivers for the transmission and reception of data.

AT89S51/52

Atmel AT89S51/52 microcontroller has an integrated **UART** module for carrying serial communication. Serial communication makes use of asynchronous mode of operation. Serial port is defined as an interface between the PC and a device for transfer of data. **AT89S51/52** with a serial port will allow reading and writing values to and from computer. The transfer of data through a serial port is bit by bit.

4.5 ZIGBEE TRANSCEIVER

The Zigbee module provides an alternative way to transfer data without the use of wires. Zigbee transceiver is developed by Digi. It was among the first transceivers that hit the market an came in a convenient to use casing. The Zigbee uses a wireless 2.4GHz transceiver to communicate with another Zigbee Module. Furthermore, Zigbee modules are capable of communicating with more than one zigbee module. Thus, it means that a network of Zigbee modules can be created all over the place as long as they are in range.

Some features of Zigbee are:

- 802.15.4 protocol created by the IEEE foundation.
- Data rate of 250kbps.
- Can be used indoors and outdoors.
- Its low power consumption offers transmission distances to 10–100 meters line-of-sight.

4.5.1 Pin Description

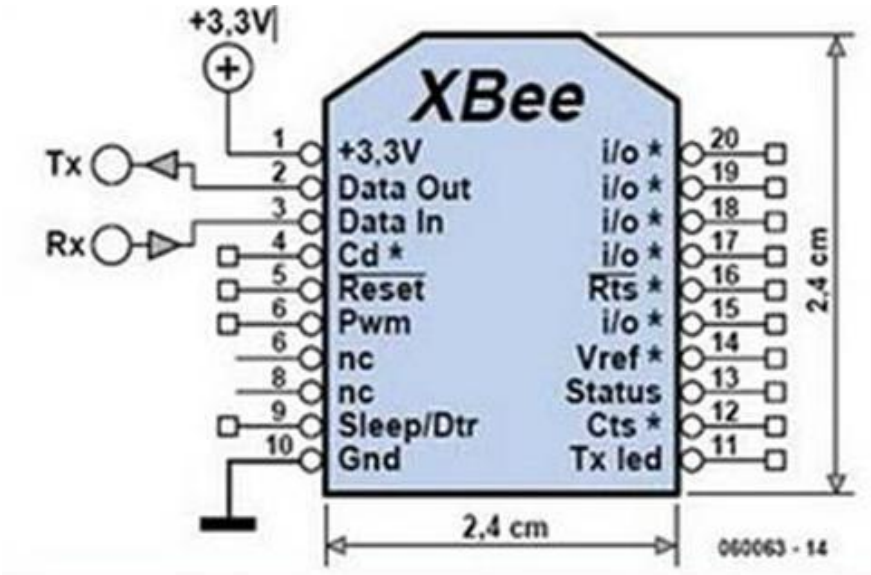


Figure 4.8: Pin Diagram

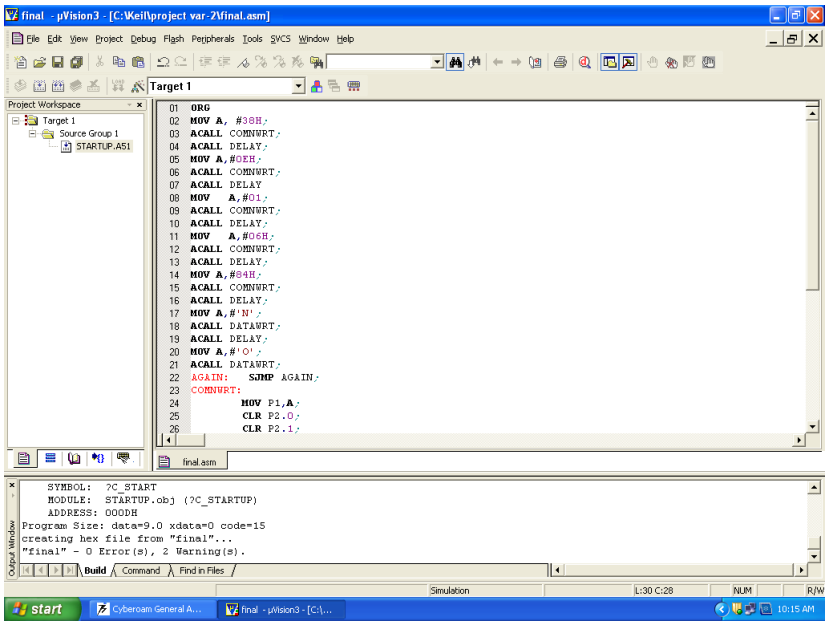
Pin Number	Name	Description
1	VCC	Power Supply
2	DOUT	UART Data Out
3	DIN/CONFIG	UART Data In
4	DO8*	Digital Output 8
5	RESET	Module Reset
6	PWM0/RSSI	PWM Output 0/RX signal strength indicator
7	PWM1	PWM Output 1
8	[reserved]	Do not connect
9	DTR/Sleep_RQ/DI8	Pin Sleep control line ordigital Input 8
10	GND	Ground
11	AD4/DIO4	Analog Input4/Digital IO4
12	CTS/DIO7	Clear to send /Digital IO7
13	ON/SLEEP	Module Status indicator
14	VREF	Voltage reference for AD inputs
15	Associate/AD5/DIO5	Associated indicator,Analog input 5/Digital IO 5
16	RTS/AD6/DIO6	Request to send/Analog input 6/ Digital IO 6
17	AD3/DIO3	Analog input 3/ Digital IO 3
18	AD2/DIO2	Analog input 2/ Digital IO 2
19	AD1/DIO1	Analog input 1/ Digital IO 1
20	AD0/DIO0	Analog input 0/ Digital IO 0

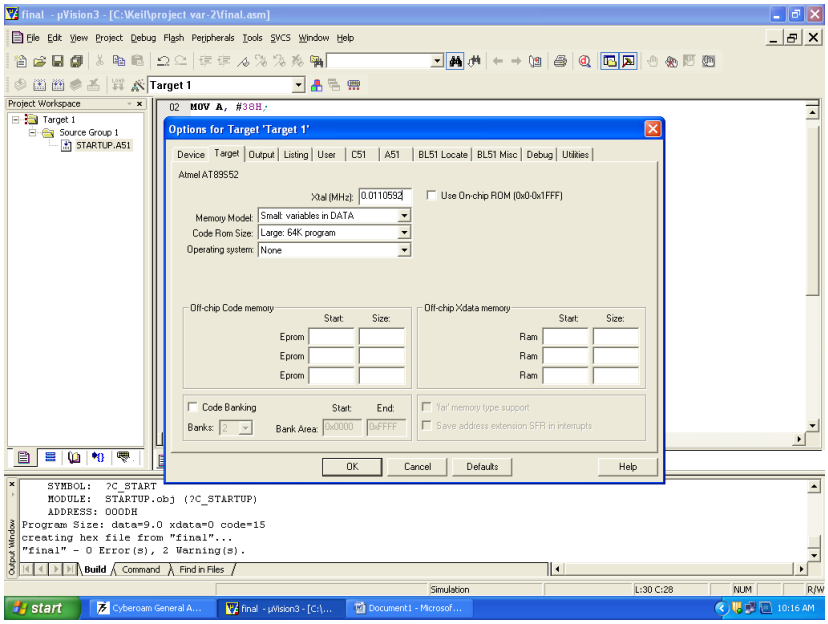
Table 4.5: Functions of pins of zigbee

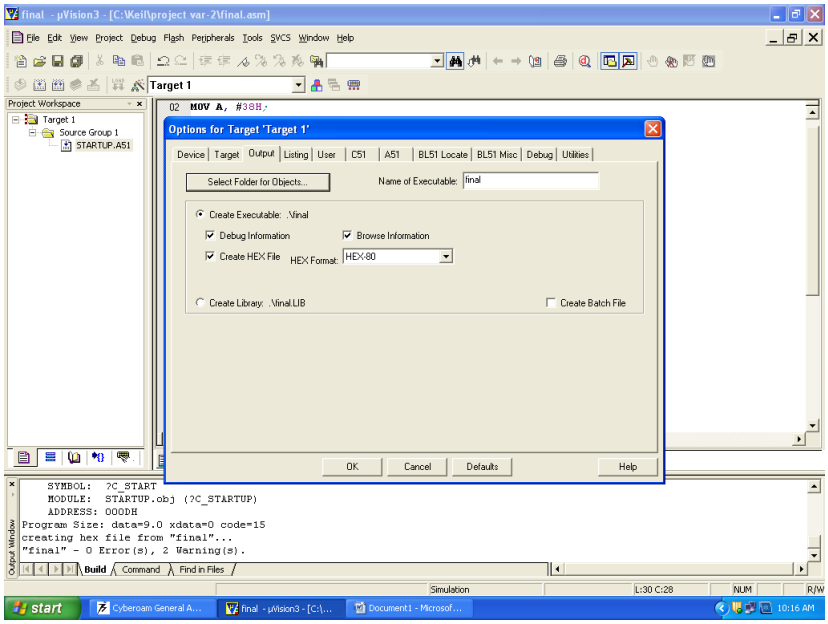
CHAPTER 5

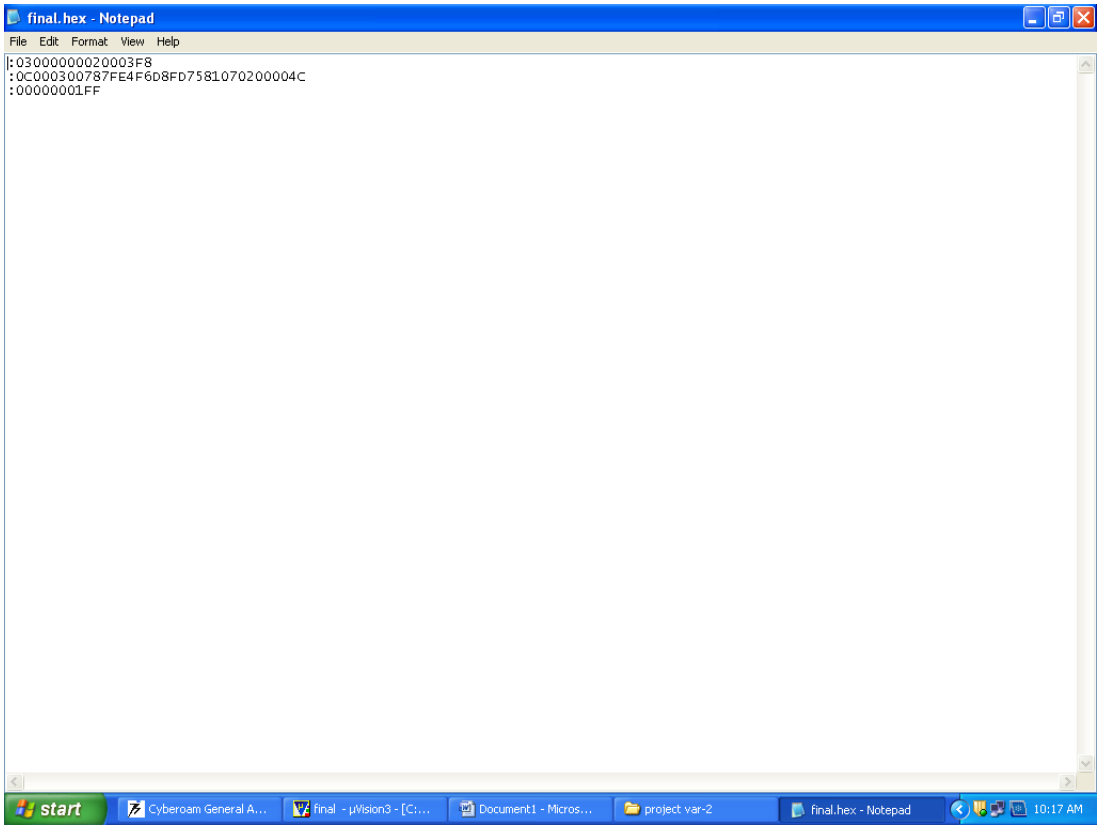
CIRCUIT SIMULATION

5.1 Creating a .HEX File




final - µVision3 - [C:\Keil\project var-2\final.asm]
Options for Target 'Target 1'
Device | Target | Output | Listing | User | C51 | A51 | BL51 Locate | BL51 Misc | Debug | Utilities
Atmel AT89S52
Xtal (MHz): 0.0110592
Use On-chip ROM (0x0-0x1FFF)
Memory Model: Small: variables in DATA
Code Rom Size: Large: 64K program
Operating system: None
Off-chip Code memory
Off-chip Xdata memory
Start: Size:
Eprom
Ram
Code Banking
Banks:
Bank Area:
OK
Cancel
Defaults
Help
SYMBOL: ?C_START
MODULE: STARTUP.obj (?C_STARTUP)
ADDRESS: 000DH
Program Size: data=9.0 xdata=0 code=15
creating hex file from "final"...
"final" - 0 Error(s), 2 Warning(s).
Build
Command
Find in Files
Simulation
L:30 C:28
NUM
start
10:16 AM


final - µVision3 - [C:\Keil\project var-2\final.asm]
Options for Target 'Target 1'
Device | Target | Output | Listing | User | C51 | A51 | BL51 Locate | BL51 Misc | Debug | Utilities
Select Folder for Objects...
Name of Executable: final
Create Executable: .\final
Debug Information
Browse Information
Create HEX File
HEX Format: HEX-80
Create Library: .\final.LIB
Create Batch File
OK
Cancel
Defaults
Help
SYMBOL: ?C_START
MODULE: STARTUP.obj (?C_STARTUP)
ADDRESS: 000DH
Program Size: data=9.0 xdata=0 code=15
creating hex file from "final"...
"final" - 0 Error(s), 2 Warning(s).
Build
Command
Find in Files
Simulation
L:30 C:28
NUM
start
10:16 AM


final.hex - Notepad
File Edit Format View Help
:03000000020003F8
:0C000300787FE4F6D8FD7581070200004C
:00000001FF
start
Cyberoam General A...
final - µVision3 - [C:...
Document1 - Micros...
project var-2
final.hex - Notepad
10:17 AM

CHAPTER-6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

Today's world is becoming technologically strong and advanced with each passing day. Manual paper work is being eliminated at every sphere of life, be it at work or home.Electronic Notice Boards have revolutionized the way of spreading information amongst the crowd. Organizations have started using electronic notice boards for displaying notices and other important information. Even advertisements are being displayed digitally using LEDs at road junctions,crossings and shopping malls. In railway station and bus stands everything from ticket information to platform number is displayed on digital moving displays.

Another aspect which is highly eminent now a days is data security. Data can be easily hacked or copied which reduced the quality of communication and increases the risk of information leak.

In this project we see electronic notice board which store particular information and displays the particular information only till it is provided with new information.It is not stored permanently.

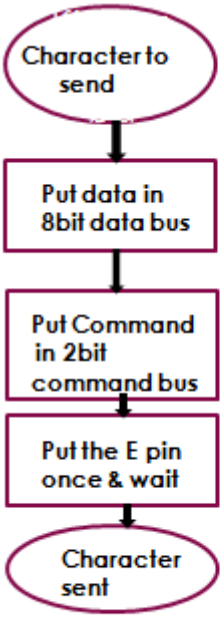
The outcome of this project is an embedded system providing wireless transmission from one point to the other via Zigbeetransceiver.This system is a reliable and fast medium for data transmission. Apart from the wide applications already mentioned, it has scope for further enhancements in the field of embedded systems where telecommunication is a vital part of the system and thereby holds the power to change the face of present communication systems.

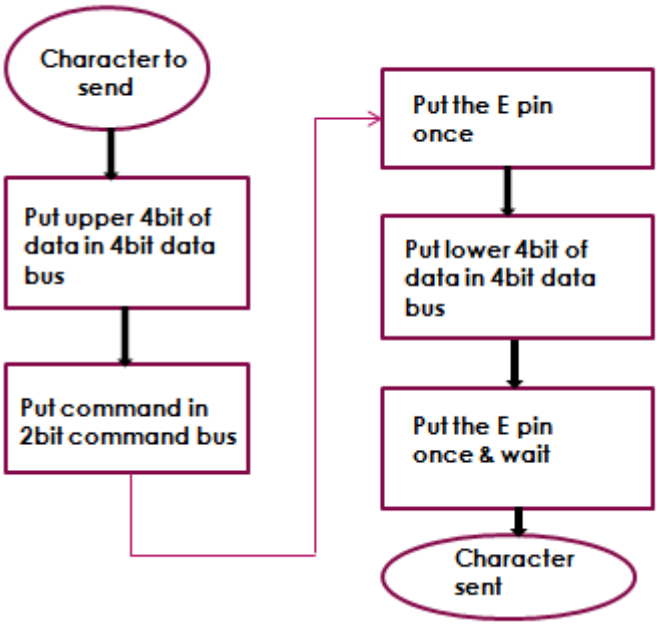
6.2 Future work

- Alphanumeric LCDs have a limitation on size as well as number of characters. They can be replaced with large LED display boards which are not only eyecatching but display characters in a moving fashion one after the other.
- A commercial model should be able to display more than one message at a time. Currently in our project we are using onboard RAM memory to save a single message. To overcome this shortcoming we can interface an EEPROM to save messages. This not only allows more than one message to be displayed at a time but also allows to retrieve messages from EEPROM even after a power failure.
- In our project we have connected one receiver with a transmitter but zigbee can have upto 32000 nodes, so we can connect more than one receiver.This can have application in various public places where the receivers can be positioned at various locations according to the needs.

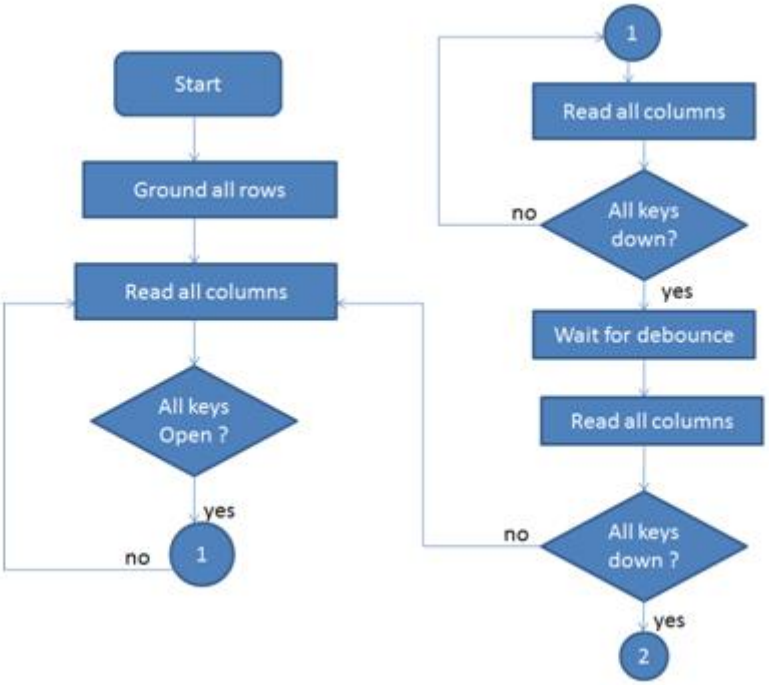
APPENDIX

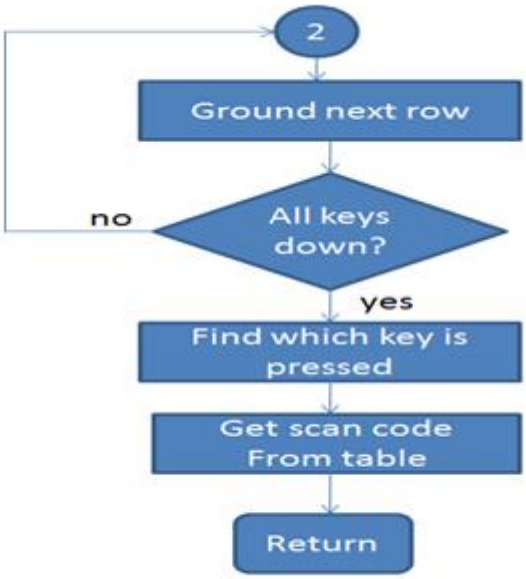
Flow chart for LCD





Flow chart for Keyboard





XBee RF Modules

The XBee and XBee-PRO RF Modules were engineered to meet IEEE 802.15.4 standards and support the unique needs of low-cost, low-power wireless sensor networks. The modules require minimal power and provide reliable delivery of data between devices. The modules operate within the ISM 2.4 GHz frequency band and are pin-for-pin compatible with each other.

Key Features

1. Long Range Data Integrity XBee

• Indoor/Urban: up to 30 m

• Outdoor line-of-sight: up to 90 m

• Transmit Power: 1 mW (0 dBm)

• Receiver Sensitivity: -92 dB

2. Low Power XBee

• TX Peak Current: 45 mA (@3.3 V)

• RX Current: 50 mA (@3.3 V)

• Power-down Current: < 10 µA

Specifiactions:

Specification	XBee	XBee-PRO
Performance		
Indoor/Urban Range	Up to 100 ft (30 m)	Up to 300 ft. (90 m), up to 200 ft (60 m) International variant
Outdoor RF line-of-sight Range	Up to 300 ft (90 m)	Up to 1 mile (1600 m), up to 2500 ft (750 m) international variant
Transmit Power Output (software selectable)	1mW (0 dBm)	63mW (18dBm)* 10mW (10 dBm) for International variant
RF Data Rate	250,000 bps	250,000 bps
Serial Interface Data Rate (software selectable)	1200 bps - 250 kbps (non-standard baud rates also supported)	1200 bps - 250 kbps (non-standard baud rates also supported)
Receiver Sensitivity	-92 dBm (1% packet error rate)	-100 dBm (1% packet error rate)
Power Requirements		
Supply Voltage	2.8 – 3.4 V	2.8 – 3.4 V
Transmit Current (typical)	45mA (@ 3.3 V)	250mA (@3.3 V) (150mA for international variant) RPSMA module only: 340mA (@3.3 V) (180mA for international variant)
Idle / Receive Current (typical)	50mA (@ 3.3 V)	55mA (@ 3.3 V)
Power-down Current	< 10 µA	< 10 µA
General		
Operating Frequency	ISM 2.4 GHz	ISM 2.4 GHz
Dimensions	0.960" x 1.087" (2.438cm x 2.761cm)	0.960" x 1.297" (2.438cm x 3.294cm)
Operating Temperature	-40 to 85° C (industrial)	-40 to 85° C (industrial)
Antenna Options	Integrated Whip, Chip or U.FL Connector, RPSMA Connector	Integrated Whip, Chip or U.FL Connector, RPSMA Connector
Networking & Security		
Supported Network Topologies	Point-to-point, Point-to-multipoint & Peer-to-peer	
Number of Channels (software selectable)	16 Direct Sequence Channels	12 Direct Sequence Channels
Addressing Options	PAN ID, Channel and Addresses	PAN ID, Channel and Addresses
Agency Approvals		
United States (FCC Part 15.247)	OUR-XBEE	OUR-XBEEPRO
Industry Canada (IC)	4214A XBEE	4214A XBEEPRO

Electrical Characteristics:

Electrical Characteristics

Table 1-03. DC Characteristics (VCC = 2.8 - 3.4 VDC)

Symbol	Characteristic	Condition	Min	Typical		Max	Unit
V_{IL}	Input Low Voltage	All Digital Inputs	-	-		0.35 * VCC	V
V_{IH}	Input High Voltage	All Digital Inputs	0.7 * VCC	-		-	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, VCC >= 2.7 V	-	-		0.5	V
V_{OH}	Output High Voltage	I_{OH} = -2 mA, VCC >= 2.7 V	VCC - 0.5	-		-	V
I_{IN}	Input Leakage Current	V_{IN} = VCC or GND, all inputs, per pin	-	0.025		1	µA
I_{OZ}	High Impedance Leakage Current	V_{IN} = VCC or GND, all I/O High-Z, per pin	-	0.025		1	µA
TX	Transmit Current	VCC = 3.3 V	-	45 (XBee)	215, 140 (PRO, Int)	-	mA
RX	Receive Current	VCC = 3.3 V	-	50 (XBee)	55 (PRO)	-	mA
PWR-DWN	Power-down Current	SM parameter = 1	-	< 10		-	µA

Table 1-04. ADC Characteristics (Operating)

Symbol	Characteristic	Condition	Min	Typical	Max	Unit
V_{REFH}	VREF - Analog-to-Digital converter reference range		2.08	-	V_{DDAD}*	V
I_{REF}	VREF - Reference Supply Current	Enabled	-	200	-	µA
		Disabled or Sleep Mode	-	< 0.01	0.02	µA
V_{INDC}	Analog Input Voltage[1]		V_{SSAD} - 0.3	-	V_{DDAD} + 0.3	V

1. Maximum electrical operating range, not valid conversion range.
* V_{DDAD} is connected to VCC.

Table 1-05. ADC Timing/Performance Characteristics[1]

Symbol	Characteristic	Condition	Min	Typical	Max	Unit
R_{AS}	Source Impedance at Input[2]		-	-	10	kΩ
V_{AIN}	Analog Input Voltage[3]		V_{REFL}		V_{REFH}	V
RES	Ideal Resolution (1 LSB)[4]	2.08V ≤ V_{DDAD} ≤ 3.6V	2.031	-	3.516	mV
DNL	Differential Non-linearity[5]		-	±0.5	±1.0	LSB
INL	Integral Non-linearity[6]		-	±0.5	±1.0	LSB
E_{ZS}	Zero-scale Error[7]		-	±0.4	±1.0	LSB
F_{FS}	Full-scale Error[8]		-	±0.4	±1.0	LSB
E_{IL}	Input Leakage Error[9]		-	±0.05	±5.0	LSB
E_{TU}	Total Unadjusted Error[10]		-	±1.1	±2.5	LSB

RF Module Operation Serial Communications TheXbee RF Modules interface to a host device through a logic-level asynchronous serial port. Through its serial port, the module can communicate with any logic and voltage compatible UART; or through a level translator to any serial device (For example: Through a Digi proprietary RS-232 or USB interface board).

UART Data Flow

Serial Data enters the module UART through the DI pin (pin 3) as an asynchronous serial signal. The signal should idle high when no data is being transmitted. Each data byte consists of a start bit (low), 8 data bits (least significant bit first) and a stop bit (high). The following figure illustrates the

serial bit pattern of data passing through the module. Serial communications depend on the two UARTs (the microcontroller's and the RF module's) to be configured with compatible settings (baud rate, parity, start bits, stop bits, data bits). The UART baud rate and parity settings on the XBee module can be configured with the BD and SB commands, respectively.

Transparent Operation By default, XBeeRF Modules operate in Transparent Mode. When operating in this mode, the modules act as a serial line replacement - all UART data received through the DI pin is queued up for RF transmission. When RF data is received, the data is sent out the DO pin. Serial-to-RF Packetization Data is buffered in the DI buffer until one of the following causes the data to be packetized and transmitted: If the module cannot immediately transmit (for instance, if it is already receiving RF data), the serial data is stored in the DI Buffer. The data is packetized and sent at any RO timeout or when 100 bytes (maximum packet size) are received. If the DI buffer becomes full, hardware or software flow control must be implemented in order to prevent overflow (loss of data between the host and module).

API Operation API (Application Programming Interface) Operation is an alternative to the default Transparent Operation. The frame-based API extends the level to which a host application can interact with the networking capabilities of the module. When in API mode, all data entering and leaving the module is contained in frames that define operations or events within the module.

Transmit Data Frames (received through the DI pin (pin 3)) include:

• RF Transmit Data Frame

• Command Frame (equivalent to AT commands)

Receive Data Frames (sent out the DO pin (pin 2)) include:

• RF-received data frame

• Command response

• Event notifications such as reset, associate, disassociate, etc. The API provides alternative means of configuring modules and routing data at the host application layer. A host application can send data frames to the module that contain address and payload information instead of using command mode to modify addresses. The module will send data frames to the application

containing status packets; as well as source, RSSI and payload information from received data packets.

MAX232 Datasheet:

MAX232x Dual EIA-232 Drivers/Receivers

1 Features

- Meets or Exceeds TIA/EIA-232-F and ITU Recommendation V.28
- Operates From a Single 5-V Power Supply With 1.0-µF Charge-Pump Capacitors
- Operates up to 120 kbit/s
- Two Drivers and Two Receivers
- ±30-V Input Levels
- Low Supply Current: 8 mA Typical
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
- Upgrade With Improved ESD (15-kV HBM) and 0.1-µF Charge-Pump Capacitors is Available With the MAX202 Device

2 Applications

- TIA/EIA-232-F
- Battery-Powered Systems
- Terminals
- Modems
- Computers

3 Description

The MAX232 device is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels.

Device Information(1)

ORDER NUMBER	PACKAGE (PIN)	BODY SIZE
MAX232x	SOIC (16)	9.90 mm × 3.91 mm
	SOIC (16)	10.30 mm × 7.50 mm
	PDIP (16)	19.30 mm × 6.35 mm
	SOP (16)	10.3 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Input Supply voltage range(2)		–0.3	6	V
V_{S+}	Positive output supply voltage range		V_{CC} – 0.3	15	V
V_{S-}	Negative output supply voltage range		–0.3	–15	V
V_I	Input voltage range	T1IN, T2IN	–0.3	V_{CC} + 0.3	V
		R1IN, R2IN		±30	
V_O	Output voltage range	T1OUT, T2OUT	V_{S-} – 0.3	V_{S+} + 0.3	V
		R1OUT, R2OUT	–0.3	V_{CC} + 0.3	
	Short-circuit duration	T1OUT, T2OUT	Unlimited		
T_J	Operating virtual junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (T1IN,T2IN)		2			V
V_{IL}	Low-level input voltage (T1IN, T2IN)				0.8	V
R1IN, R2IN	Receiver input voltage				±30	V
T_A	Operating free-air temperature	MAX232	0		70	°C
		MAX232I	–40		85	

7.4 Thermal Information

THERMAL METRIC(1)		MAX232xD SOIC 16 PINS	MAX232xDW SOIC wide 16 PINS	MAX232xN PDIP 16 PINS	MAX232xNS SOP 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	57	67	64	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics — Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5V, all outputs open, T_A = 25°C		8	10	mA

(1) Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

7.6 Electrical Characteristics — Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND	5	7		V
V_{OL}	Low-level output voltage(3)	T1OUT, T2OUT	R_L = 3 kΩ to GND		–7	–5	V
r_O	Output resistance	T1OUT, T2OUT	V_{S+} = V_{S-} = 0, V_O = ±2 V	300			Ω
I_{OS}(4)	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5 V, V_O = 0 V		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0			200	µA

(1) Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
(4) Not more than one output should be shorted at a time.

7.7 Electrical Characteristics — Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	R1OUT, R2OUT	I_{OH} = –1 mA	3.5			V
V_{OL}	Low-level output voltage(3)	R1OUT, R2OUT	I_{OL} = 3.2 mA			0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	R1IN, R2IN	V_{CC} = 5 V	0.2	0.5	1	V
r_I	Receiver input resistance	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C	3	5	7	kΩ

(1) Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

7.8 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(1)	MAX	UNIT
SR	Driver slew rate	RL = 3 kΩ to 7 kΩ, see Figure 4			30	V/µs
SR(t)	Driver transition region slew rate	see Figure 5		3		V/µs
	Data rate	One TOUT switching		120		kbit/s
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	TTL load, see Figure 3		500		ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	TTL load, see Figure 3		500		ns

(1) Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

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