CMOS COMPATIBLE ANALOG FILTERS BASED ON DIFFERENTIAL VOLTAGE CURRENT CONVEYOR

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CERTIFICATE

This is to certify that the work entitled, "CMOS Compatible Analog Filters based on Differential Voltage Current Conveyor" submitted by Vivek Verma and Girish Garg in partial fulfillment for the award of degree of Bachelors of Technology in Electronics and Communication Engineering of Jaypee University of Information Technology has been carried out under my supervision. This work has not been submitted partially or wholly to any other University or Institute for the award of this or any other degree or diploma.

Mr. Jitendra Mohan

Prof. S.V. Bhooshan

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Vivek Verma

Girish Garg

ABSTRACT

This project presents new filter circuits, i.e. first order all-pass, second order circuits based on Differential Voltage Current Conveyor (DVCC). A DVCC has advantages of both the second generation current conveyor (CCII) (such as large signal bandwidth, greater linearity, wide dynamic range) and differential difference amplifier (DDA) (such as high input impedance and arithmetic operational capability). A new first order all-pass filter in current mode operation using the DVCC is proposed. The novelty of the configuration is that the DVCC supplies high input impedances for applications requesting differential or floating inputs.

A new current mode biquadratic filter using DVCC filter and all grounded passive elements is proposed. The circuit can simultaneously realize low-pass and high-pass filter functions without changing the circuit topology and elements. It has the possibility of independent adjustment of ω_o without disturbing ω_o/q.

A new high input impedance voltage mode biquadratic filter with one input terminal and three output terminals is proposed. The proposed circuit uses three DVCCs, two resistors and two grounded capacitors. The proposed circuit realizes the filter functions low-pass, band-pass and notch filter simultaneously without changing passive elements.

The feasibility and accuracy of the proposed circuit are verified well by using PSPICE simulation.

CONTENTS

CHAPTER 1

INTRODUCTION TO DVCC

1.1 MOTIVATION

The current mode circuits have received significant attention due to their particular advantages as compared with voltage mode circuits [1-4]. They offer the designer several salient features as inherently wide bandwidth, greater linearity, wider dynamic range, simple circuitry and low power consumption. At present, a number of current-mode circuit techniques, such as current conveyors (CCs) and four terminal float nullors (FTFNs) have been developed.

In this technique the current conveyors have proved to be functionally flexible and versatile current-mode building block. Second generation current conveyors (CCIIs) have found wide use in variety of realizations of active network elements and current-mode circuits.

For voltage-mode circuits the electrical variables, for example, the input-output variables are voltage where as in current-mode circuits these quantities are selected as current. The classical voltage amplifier with its high impedance input and low impedance output is a suitable element for voltage mode circuits. The current conveyor with its one high impedance (ideally zero) input and one high impedance output is suitable element for both voltage -mode and current-mode circuits.

Current-mode circuits are used instead of voltage mode circuits for wide variety of applications [4-6, 14, 15]. The reason is that in voltage mode circuits the high valued resistors with parasitic capacitances create a dominant pole at relatively low frequency, which limits the bandwidth.

In general the node impedances in current-mode circuits are low and the voltage swings are small. Thus the time constant is reduced and also the time required for charging and discharging a parasitic capacitor is kept

small. Hence the slew rate for current mode circuits is significantly high. They are well suited to work at higher frequencies and thus are often used in communication circuits. Furthermore, current-mode circuits are suitable for integration with the CMOS technology and thus have become more and more attractive in electronic circuit design in recent years.

The differential voltage current conveyor (DVCC) is an extension of the second-generation current conveyor (CCII) [7, 16]. Recently, the CCII has been realized using MOS transistors, with the intention to integrate the different CCII circuit applications on one chip. The CCII proves to be a versatile building block that can be used to implement a variety of high-performance circuits which are simple to construct. The CCII has a disadvantage that only one of the input terminals has high input impedance (the Y terminal). This disadvantage becomes evident when the CCII is required to handle differential signals, as in the case of an instrumentation amplifier. The design of such an amplifier requires two or more CCIIs. A basic section used in realizing floating input applications from CCIIs is given in. Using such a circuit to realize an instrumentation amplifier results in an amplifier structure that has the advantage of a high CMRR (even at high frequencies) without the need for an accurately matched resistor network. The circuit given in uses two CCIIs and a floating resistor to provide floating input handling capability. Moreover, the floating resistor is connected between the X terminals of the two CCIIs. As each **X** terminal has an output resistance R, the effective resistance between the two X terminals is R+2Rx that is the error caused by the nonzero X terminal resistance is doubled. In this paper the differential voltage current conveyor (DVCC) building block is proposed. The DVCC is a novel building block specially defined to handle differential signals.

1.2 DIFFERENTIAL VOLTAGE CURRENT CONVEYOR DESCRIPTION

The DVCC is a five-port building block which is shown symbolically in figure 1.1 and defined by the following matrix equation:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \qquad (1.1)$$

$$V_X = V_{Y1} - V_{Y2} \qquad (1.2)$$

$$I_{Y1} = I_{Y2} = 0 \qquad (1.3)$$

$$I_{Z1} = I_X \qquad (1.4)$$

$$I_{Z2} = -I_X \qquad (1.5)$$

Where the plus and minus signs indicate both DVCC+ and DVCC- realization simultaneously.

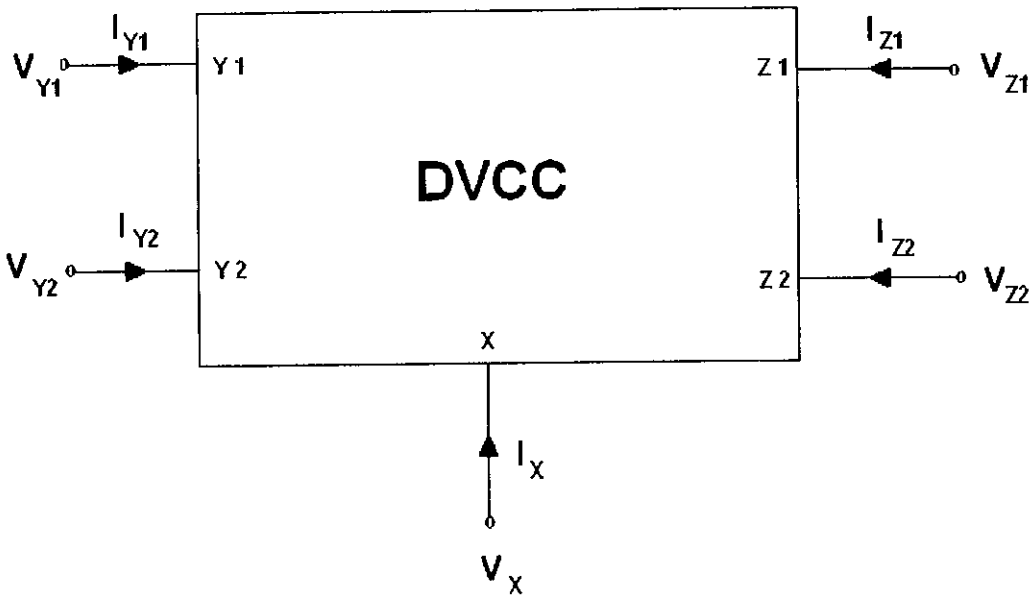

Fig 1.1 Symbol of DVCC

1.2.1 CMOS IMPLEMENTATION OF DVCC

The differential voltage conveying action of the circuit is based on the differential pairs M1, M2 and M3, M4.The current mirror formed by transistors M7 and M8 forces the sum of the drain currents of M1 and M3 to be equal to the sum of the drain currents of M2 and M4, hence

$$I_1 - I_2 = I_4 - I_3 \qquad (1.6)$$

Therefore,

$$V_{G1} - V_{G2} = V_{G4} - V_{G3} \qquad (1.7)$$

$$V_X = V_{Y1} - V_{Y2} \qquad (1.8)$$

Transistors M9 and M12 provide the necessary feedback action to make the voltage V, independent of the current drawn from the terminal X. It is worth noting that Equation 1.8 is valid for large signals. The current through terminal X is conveyed to the Z1 terminal by the current mirrors consisting of transistors M9, M10 and M12, M13. By using extra current mirrors, the current is conveyed in an inverted manner to the Z2 terminal as described before.

The operation of this circuit is insensitive to the threshold voltage variation caused by the body effect. All the PMOS transistors have sources which are connected to the positive supply rail, while all NMOS transistors, except M1, M2, M3 and M4, have sources connected to the negative supply rail. This causes no variation in the threshold voltage because the source to body voltage is maintained equal to zero at all times. Although the sources of transistors M1 and M2 are not connected to the body, their operation is still unaffected by the body effect because they form a differential pair, and, hence, have the same source voltage. This causes equal variation in the

threshold voltage of M1 and M2, and, hence, the two threshold voltages cancel out. The same is true for the differential pair transistors M3 and M4. All the MOS transistors operate in saturation region and the sources are connected to the substrate. The input transconductance elements are realized with two differential stages (M1-M2 and M3-M4). The high-gain stage is composed of a current mirror (M7-M8), which converts the differential current to a single ended output current (M9).

We performed PSPICE simulations of the circuit (shown in Fig. 1.2) using 0.35μ level-3 model parameters obtained through MOSIS. The aspect ratios of the transistors used in the simulation are given in Table 1. The supply voltages are adjusted to ± 2.5 Volts. The biasing current I_b is chosen as 200 μA.

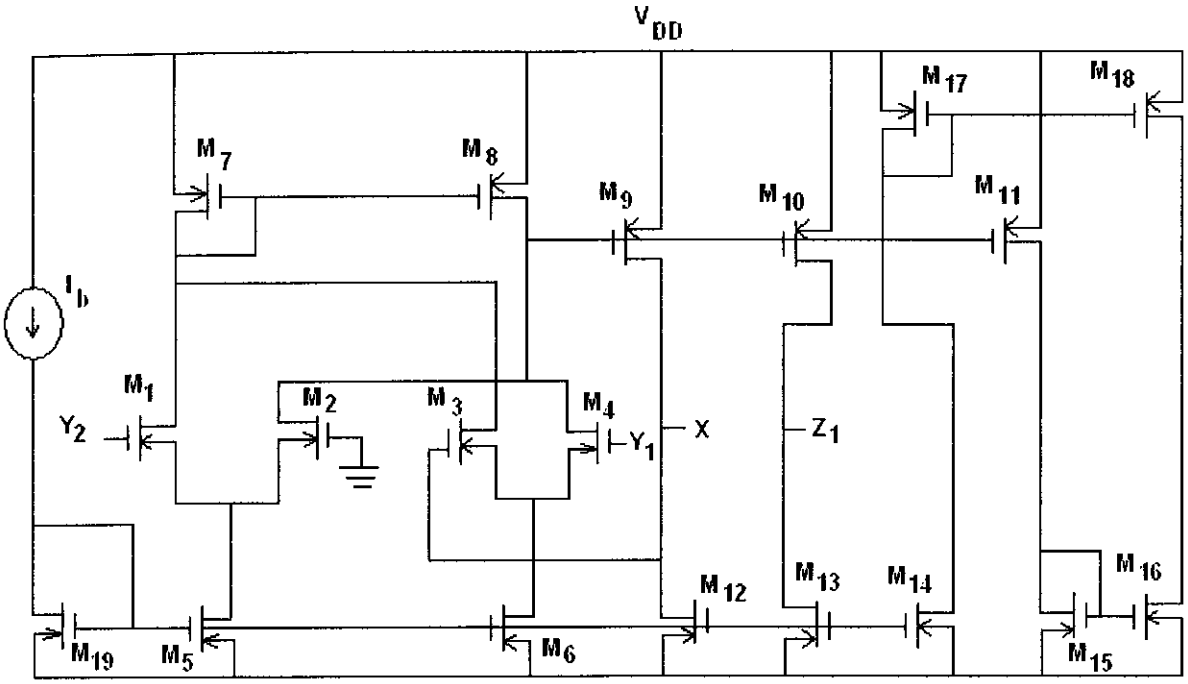

Fig 1.2 CMOS Realization of DVCC

CHAPTER 2

DVCC BASED FIRST ORDER ALL-PASS FILTER

First-order all-pass filters using current conveyors are an important class of analogue signal processing circuits that have been extensively researched in the literature [8-10, 14, 15]. The popularity of this circuit function is attributed to its utility in communication and instrumentation systems [1-3], for instance, as a phase equalizer, phase shifter or for realizing quadrature oscillators, bandpass filters etc.

2.1 FIRST-ORDER ALL-PASS FILTER

The proposed first-order all-pass filter is shown in Figure 2.1. Selecting R_2=2R_1 the analysis of the proposed circuit in figure 2.1 for the current transfer function yields

$$G(s)=\frac{I_{out}}{I_{in}}(s)=-\frac{R_2}{2R_3}\frac{1-sCR_2}{1+sCR_2} \qquad (2.1)$$

The gain of the filter is found as

$$K_O=-\frac{R_2}{2R_3} \qquad (2.2)$$

And the filter has the following phase response

$$\varphi(\omega)=180^0-2\tan^{-1}(\omega R_2C) \qquad (2.3)$$

From equation (2.3) it can be seen that the circuit yields a phase shift from 180^0 to 0^0. The pole frequency of the circuit is found as

$$f_p=\frac{1}{2\Pi R_2C} \qquad (2.4)$$

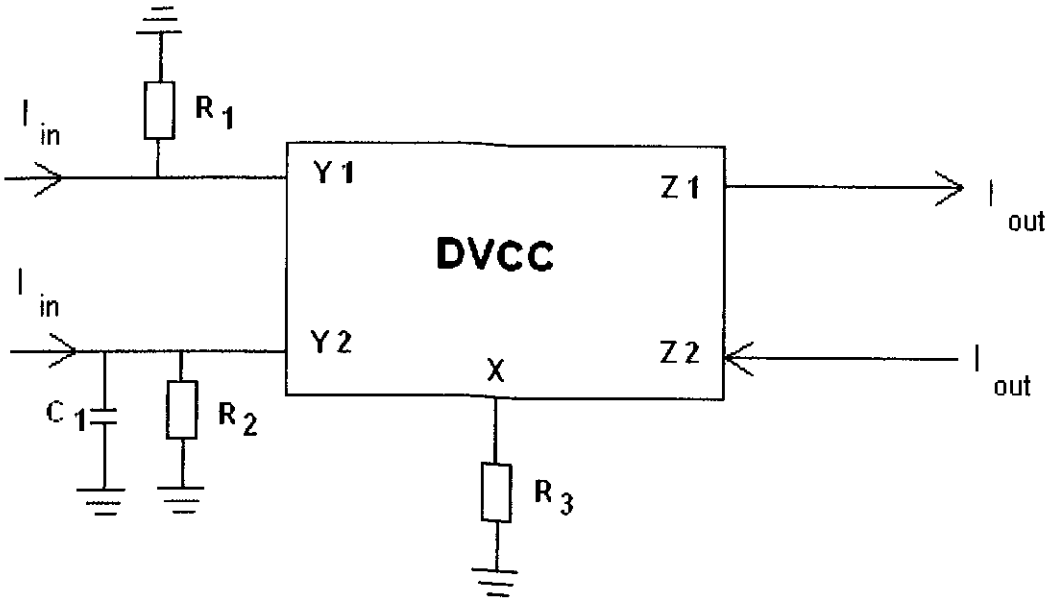

Figure 2.1 DVCC based first order all-pass filter

From equations (2.2), (2.3) and (2.4) one can realize that the gain is independently adjustable by changing R3 without disturbing the phase response and pole frequency of the filter.

The sensitivities of the parameter f_p with respect to R_1, R_2, and C can be expressed as

$$S_{R_1}^{f_p} = S_{R_2}^{f_p} = S_C^{f_p} = -1 \qquad (2.5)$$

Which are no more than unity in magnitude.

2.2. SIMULATION RESULTS

The Figure 2.1 was simulated using the CMOS implementation (Fig. 1.2) of DVCC with CMOS 0.35 μm device parameters and the W/L ratios, given in Table 1(Appendix). The supply voltage is adjusted to $\pm$ 2.5 Volts. The biasing current I_b is chosen as $200\,\mu A$. The proposed configuration is designed to realize a first-order all pass filter with a natural frequency of 796 kHZ and a gain of -1 by choosing R_1=10k, R_2=20k, R_3=10k, and C_1=10pF. The magnitude and the phase responses obtained from the simulation of the proposed filter circuit are given in Figure 2.2.

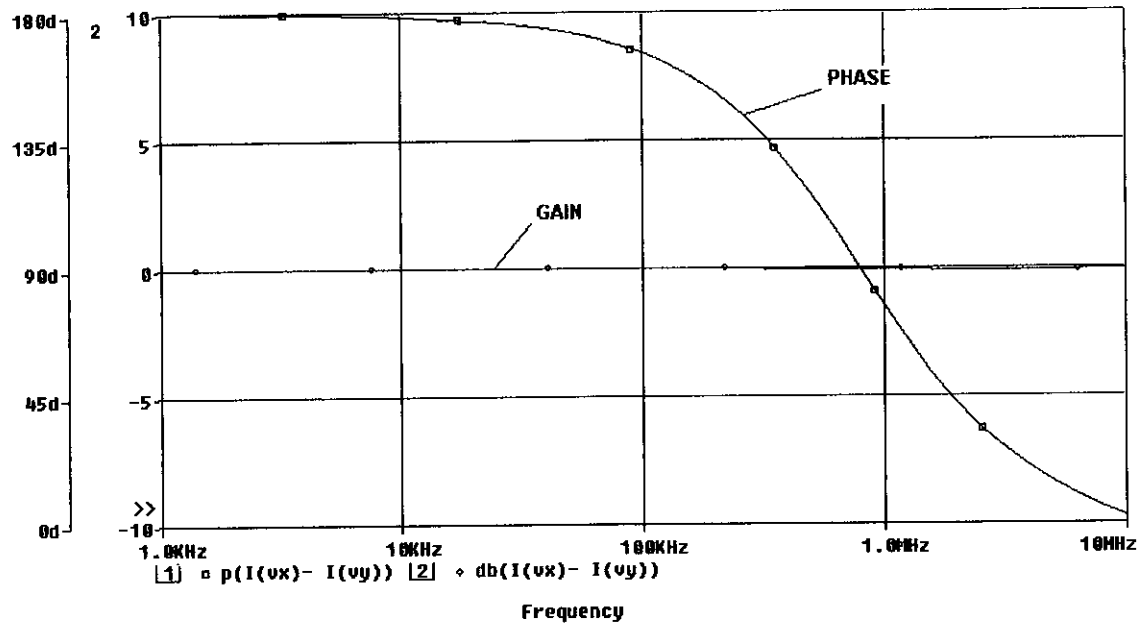

Figure 2.2 Simulation Results for first-order all-pass filter

CHAPTER 3

CURRENT MODE DVCC BASED BIQUADRATIC FILTER

Current-mode circuits have been receiving considerable attention owing to their potential advantages such as wider bandwidth, greater linearity, higher slew rate, wider dynamic range, simple circuitry and low power consumption compared to voltage-mode circuits [4]. Current-mode filters have been found wide applications instrumentation, analogue signal processing, automatic control and communication systems. The advantages in the realization of current-mode filters using current conveyors have received significant attention [5]. Although, the CCII can be used to implement many high performance circuits, it has a crucial disadvantage of having only one high input voltage terminal (Y terminal). When it is required to handle differential or floating inputs, this disadvantage becomes evident. Considering drawbacks of CCIIs, a new building block called a differential difference current conveyor (DDCC) was made. A novel differential voltage current conveyor (DVCC) building block was introduced [7].

In this chapter, a current mode biquadratic filter using two DVCCs and all-grounded five passive elements. PSPICE simulation of the CMOS DVCC universal filter is performed to demonstrate the results. The obtained simulation results are compared with the theoretical results of the filter.

3.1 PROPOSED CURRENT MODE BIQUADRATIC FILTER

The implemented current-mode biquadratic filter is illustrated in Figure 3.1. Using the standard DVCC characteristics defined in Chapter 1, routine analysis of the circuit yields the following current transfer functions:-

$$\frac{I_{LP}}{I_{in}} = \frac{1/C_1C_2R_1R_3}{s^2 + \frac{s}{C_2R_2} + \frac{1}{C_1C_2R_1R_3}} \tag{3.1}$$

$$\frac{I_{HP}}{I_{in}} = \frac{s^2}{s^2 + \frac{s}{C_2R_2} + \frac{1}{C_1C_2R_1R_3}} \tag{3.2}$$

Where the pole natural frequency and pole quality factor of the implemented filter are expressed as:-

$$\omega_O = \sqrt{\frac{1}{C_1C_2R_1R_3}} \tag{3.3}$$

$$\frac{\omega_O}{Q} = \frac{1}{C_2R_2} \tag{3.4}$$

$$Q = \frac{C_2R_2}{\sqrt{C_1C_2R_1R_3}} \tag{3.5}$$

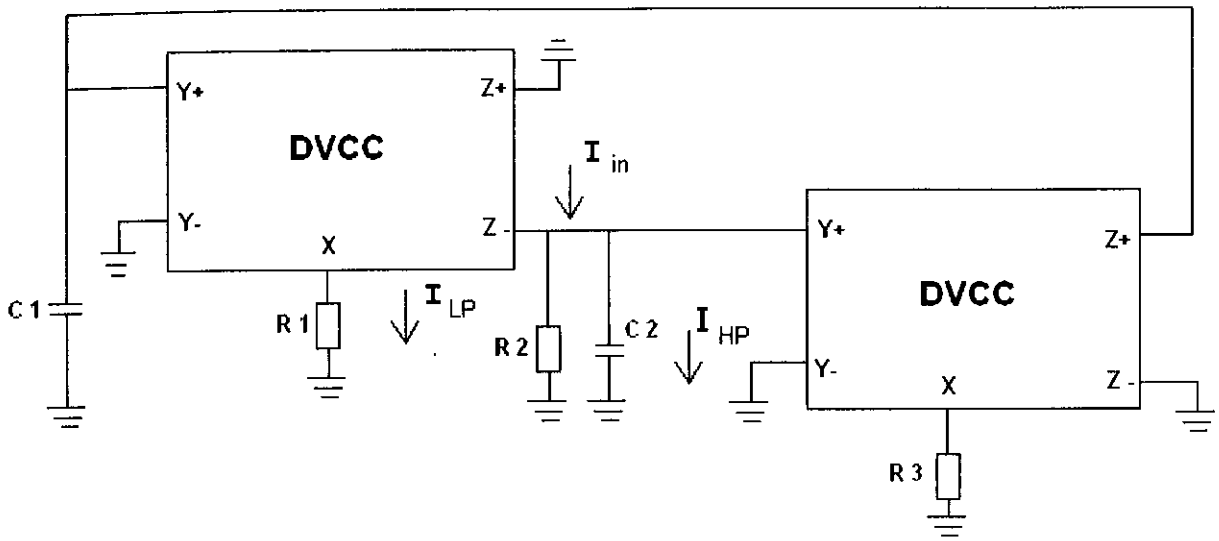

Fig. 3.1 Current mode Biquadratic filter

Thus, second-order current-mode low-pass, high-pass filter characteristics given respectively by Equations (3.1), (3.2) can be simultaneously realized without changing the circuit configuration. By adding I_{LP} & I_{HP} outputs, the transfer function can be organized giving a notch filter transfer function as follows:

$$\frac{I_{notch}}{I_{in}} = \frac{I_{HP} + I_{LP}}{I_{in}} = \frac{s^2 + 1/C_1C_2R_1R_3}{s^2 + \frac{s}{C_2R_2} + \frac{1}{C_1C_2R_1R_3}} \qquad (3.6)$$

From Equations (3.3), (3.4),(3.5), it can be seen that ω_o can be adjusted independently from ω_o/Q by changing the value of R_3. Also, the quality factor Q can be adjusted by changing the grounded resistance R_2 without affecting the pole natural frequency ω_o.

3.2 SIMULATION RESULTS

To verify theoretical analysis the implemented circuit has been simulated using PSPICE program by using 0.35 μm technology process parameters. The circuit in Fig 3.1 was used to realize lowpass, highpass and notch filters with a cutoff frequency of 255 kHz. The all-grounded passive elements of the filter were chosen as C_1=C_2=lnF, R_1=lk and R_2=R_3=0.5k. The supply voltages were taken as V_{DD}=2.5V and V_{ss}=-2.5V and I_b=200 μA. The PSPICE simulation results given in Fig 3.2 for the lowpass, highpass filter. As it can be seen from Fig 3.2, the pole natural frequency is in a good agreement with the frequency calculated using the derived analytical formula given by Equation (3.3).

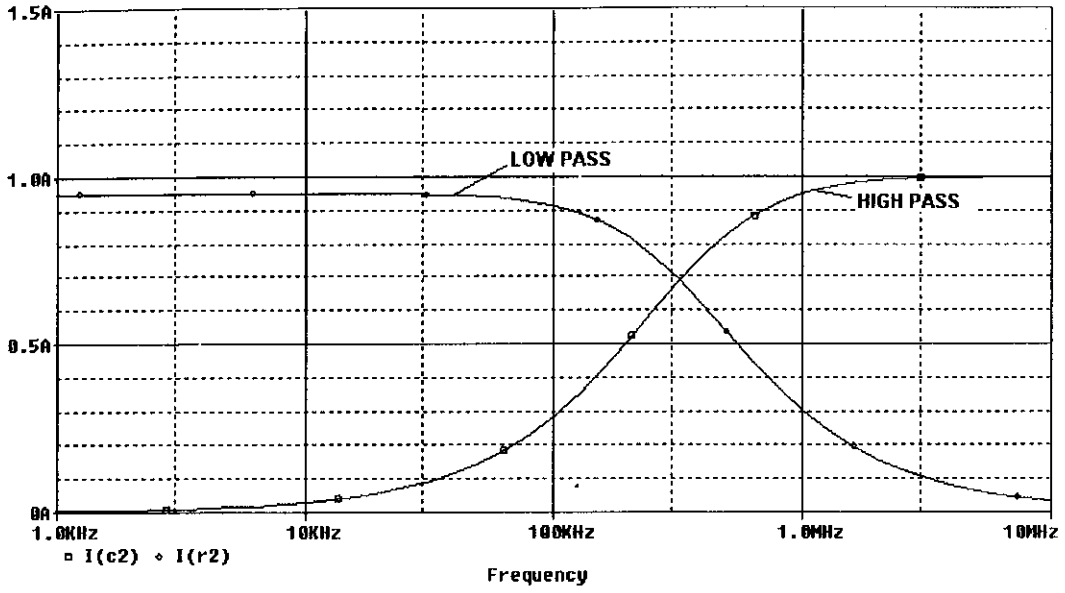

Figure 3.2 Simulated frequency response of the low-pass and high-pass filters

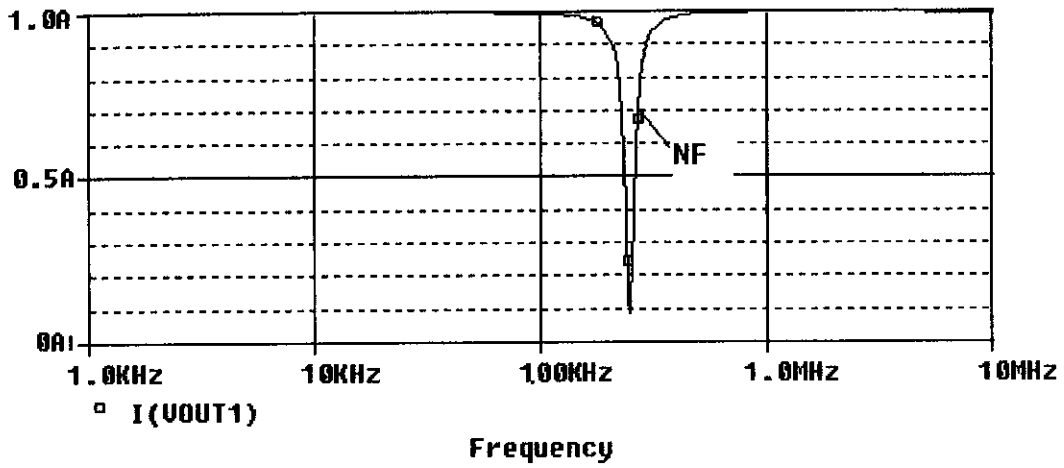

Figure 3.3 Simulated frequency response of notch filter

CHAPTER 4

VOLTAGE MODE
DVCC BASED BIQUADRATIC FILTER

Voltage-mode active filters with high input impedance are of great interest because several cells of this kind can be directly connected in cascade to implement higher-order filters [11-13]. In this chapter, a voltage-mode universal biquadratic filter with one high input impedance terminal and three output terminals is presented. The proposed circuit uses three differential voltage current conveyors (DVCCs), two grounded capacitors, and two resistors. The proposed circuit can realize all the standard filter functions: lowpass, bandpass, and notch simultaneously. The proposed circuit employs only grounded capacitors, which is ideal for IC implementation.

4.1 PROPOSED VOLTAGE MODE BIQUADRATIC FILTER

The implemented voltage-mode biquadratic filter is illustrated in Figure 4.1. Using the standard DVCC characteristics defined in Chapter 1, routine analysis of the circuit yields the following current transfer functions:-

$$\frac{V_{out3}}{V_{in}} = \frac{sC_2R_2}{s^2C_1C_2R_1R_2 + sC_2R_2 + 1} \tag{4.1}$$

$$\frac{V_{out2}}{V_{in}} = \frac{1}{s^2C_1C_2R_1R_2 + sC_2R_2 + 1} \tag{4.2}$$

$$\frac{V_{out1}}{V_{in}} = \frac{s^2 C_1 C_2 R_1 R_2 + 1}{s^2 C_1 C_2 R_1 R_2 + s C_2 R_2 + 1} \qquad (4.3)$$

Where the pole natural frequency and pole quality factor of the implemented filter are expressed as:-

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}} \qquad (4.4)$$

$$Q = \sqrt{\frac{C_1 R_1}{C_2 R_2}} \qquad (4.5)$$

Thus, the second-order voltage-mode band-pass, low-pass, and notch filter characteristics are given respectively by Equations (4.1), (4.2), and (4.3).

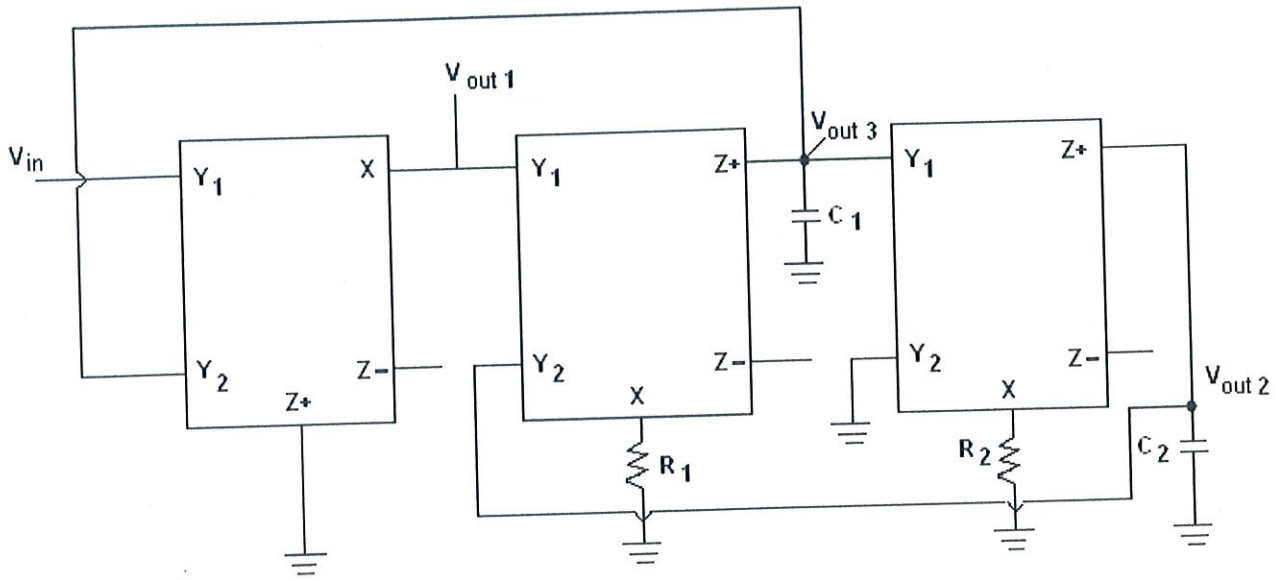

Figure 4.1 Voltage Mode DVCC based biquadtratic filter

4.2 SIMULATION RESULTS

To verify theoretical analysis the implemented circuit has been simulated using PSPICE program by using 0.35 μm technology process parameters. The circuit in Fig 4.1 was used to realize low-pass, band-pass and notch filters with a cutoff frequency of 255 kHz. The all-grounded passive elements of the filter were chosen as $C_1=C_2=10000nF$, $R_1=R_2=1\ k\Omega$. The supply voltages were taken as $V_{DD}=2.5V$ and $V_{ss}=-2.5V$ and $I_b=200\ \mu A$. The PSPICE simulation results are given in Fig 4.2 for the low-pass, band-pass, and notch filters.

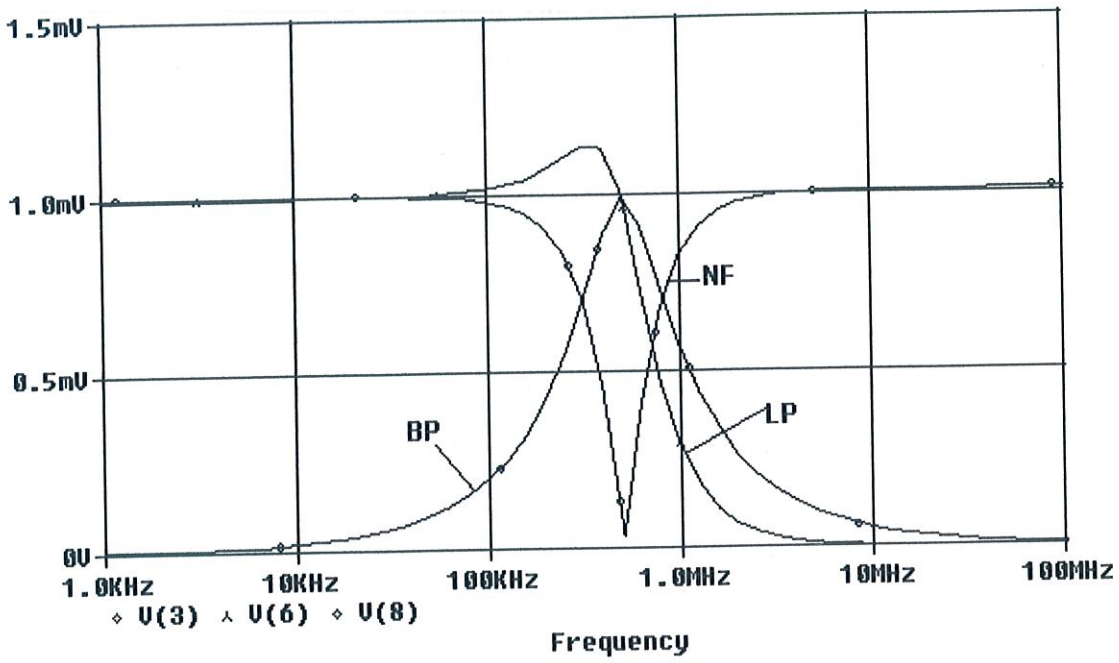

Figure 4.2 Simulation results for low-pass, band-pass and notch filters

CONCLUSION

Filter circuits based on DVCC were proposed in the work and verified through PSPICE simulations with the following main results.

In Chapter 1, a general introduction of the suggested topic is presented. CMOS implementation of DVCC is also introduced in this chapter.

In Chapter 2, a first order all-pass filter realization based on DVCC is presented. The proposed filter contains single DVCC, three resistors and one capacitor. The gain of the filter can be changed without disturbing the frequency response of the circuit. Due to the high output impedance of the circuit, it can be easily used in a cascade. The simulation results using CMOS model of DVCC verify the proposed circuit.

In Chapter 3, a current mode biquadratic filter is implemented with two DVCCs and five all grounded passive elements is introduced. The filter can simultaneously realize low-pass and high-pass filter functions without changing the topology and elements. A notch filter characteristic can also be obtained by getting a suitable output. Also, the adjustment of bandwidth and quality factor without affecting each other is possible. The PSPICE simulation result using CMOS model of DVCC verifies the proposed circuit.

In Chapter 4, a voltage mode biquadratic filter with one input terminal and three output terminals has been presented. The proposed circuit uses three DVCCs, two grounded capacitors, and two grounded resistors. Moreover, the proposed circuit has the following advantages: low active and passive sensitivity, high input impedance and no requirement for component matching.

SCOPE FOR FURTHER WORK

All the circuits presented in the work are compatible with CMOS technology. Thus, the IC fabrication of the proposed circuits is the most natural future problem. Available DVCC can be employed for realizing several functions like a four quadrant multiplier, phase shifter, equalizer, higher order filters etc. based on the proposed circuits.

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APPENDIX

Table 1: Transistor aspect ratios

Transistors	Aspect Ratios(W/L)
M1, M2, M3, M4	7.2/4.8
M7,M8	39.6/4.8
M9, M10, M11, M17, M18	111.6/3.6
M5, M6, M12, M13, M14, M15, M16	144/4.8

Table 2: 0.35 μm MOSIS model parameters

NMOS	CJSW=3.7778E-10	MJSW=0.3508721
TOX=7.9E-9	NSUB=1E17	GAMMA=0.582787
PHI=0.7	VTO=0.5445549	DELTA=0
UO=436.256	ETA=0	THETA=0.1749684
KP=2.055E-4	VMAX=8.30944E4	KAPPA=0.2574081
RSH=0.05593	NFS=1E12	TPG=1
XJ=3.E-7	LD=3.162278E-11	WD=7.046724E-8
CGDO=2.8E-10	CGSO=2.82E-10	CGBO=1E-10
CJ=1E-3	PB=0.9758533	MJ=0.3448504
PMOS	CJSW=4.8135E-10	MJSW=0.5
TOX=7.9E-9	NSUB=1E17	GAMMA=0.40838
PHI=0.7	VTO=0.7140674	DELTA=0
UO=212.231980	ETA=9.999762E-4	THETA=0.20207
KP=6.73375E-5	VMAX=1.1815E5	KAPPA=1.5
RSH=30.071245	NFS=1E12	TPG=-1
XJ=2E-7	LD=5.000001E-13	WD=1.249872E-7
CGDO=3.0E-10	CGSO=3.09E-10	CGBO=1E-10
CJ=1.41950E-3	PB=0.8152573	MJ=0.5

PROGRAM 1

```
x1 1 2 3 4 5 dvcc
i1 1 0 ac 10v
i2 2 0 ac 10v
r1 1 0 10k
r2 2 0 20k
c1 2 0 10pf
r3 3 0 10k
vx 4 0 dc 0v
vy 0 5 dc 0v

.SUBCKT DVCC 3  4 16 5 6
VDD 1 0 DC 2.5V
VSS 0 2 DC 2.5V
IB 1 12 DC 200uA
M1   17  4  19  2  NT  W=24U  L=0.35U
M2   7   0  19  2  NT  W=24U  L=0.35U
M3   17 16  8  2   NT  W=24U  L=0.35U
M4   7   3  8  2   NT  W=24U   L=0.35U
M5   17  7  1  1   PT   W=15U  L=1.5U
M6   7  17  1  1    PT  W=15U  L=1.5U
M7   12 12  2   2  NT  W=10U  L=1.5U
M8   19 12  2  2   NT  W=10U  L=1.5U
M9   8  12  2  2  NT   W=10U  L=1.5U
M10  16  7   1  1  PT  W=15U   L=1.5U
M11  16 12   2  2  NT  W=10U  L=1.5U
M12  5   7   1  1   PT  W=15U  L=1.5U
M13  5 12   2  2   NT   W=10U  L=1.5U
M14  14  7   1  1   PT  W=15U  L=1.5U
M15   9  9   1  1   PT  W=15U  L=1.5U
M16   9 12  2  2   NT  W=10U  L=1.5U
M17  14 14  2   2  NT  W=10U  L=1.5U
M18   6  9  1  1    PT  W=15U  L=1.5U
M19   6 14  2  2    NT  W=10U  L=1.5U

.MODEL NT   NMOS (LEVEL=2 TOX=7.9E-9 NSUB=1E17
+ GAMMA=0.5827871 PHI=0.7 VTO=0.5445549 DELTA=0
+ UO=436.256147 ETA=0 THETA=0.1749684 KP=2.055786E-4
+ VMAX=8.309444E4 KAPPA=0.2574081 RSH=0.0559398
+ NFS=1E12 TPG=1 XJ=3E-7 LD=3.162278E-11 WD=7.04672E-8
+ CGDO=2.82E-10 CGSO=2.82E-10 CGBO=1E-10 CJ=1E-3
+ PB=0.9758533 MJ=0.3448504 CJSW=3.777852E-10
+ MJSW=0.3508721)

.MODEL PT PMOS (LEVEL =2 TOX = 7.9E-9 NSUB=1E17
```

```
+ GAMMA=0.4083894 PHI=0.7 VTO=-0.7140674 DELTA=0
+ UO=212.2319801 ETA=9.999762E-4 THETA=0.2020774
+ KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5
+ RSH=30.0712458 NFS=1E12 TPG=-1 XJ=2E-7 LD=5.000001E-13
+ WD=1.249872E-7 CGDO=3.09E-10 CGSO=3.09E-10
+ CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 MJ=0.5
+ CJSW=4.813504E-10 MJSW=0.5)
.ENDS DVCC

.AC DEC 10 100 10000khz
.PROBE
.END
```

PROGRAM 2

```
x1 1 0 2 0 4 dvcc
x2 4 0 5 1 0 dvcc
iin 1 0 ac 1ma
r1 2 0 1k
r2 5 0 0.5k
r3 4 7 0.5k
C1 1 0 1nF
C2 4 0 1nF
vx1 7 0 dc 0v

.SUBCKT DVCC 3  4 16 5 6
VDD 1 0 DC 2.5V
VSS 0 2 DC 2.5V
IB  1 9 DC 200uA
M1   17  4  19  2  NT  W=2.4U  L=1.6U
M2   7   0  19  2  NT  W=2.4U  L=1.6U
M3   17 16   8  2  NT  W=2.4U  L=1.6U
M4   7   3   8  2  NT  W=2.4U   L=1.6U
M5   19 9 2 2   nt   W=48U  L=1.6U
M6   8 9 2 2    nt  W=48U  L=1.6U
M7   17 17 1 1   pt  W=13.2U  L=1.6U
M8   7 17 1 1    pt  W=13.2U  L=1.6U
M9   8 7 1 1    pT   W=37.2U  L=1.2U
M10  5 7 1 1   PT  W=37.2U   L=1.2U
M11  11 7 1 1   pT  W=37.2U  L=1.2U
M12   16 9 2 2   nT   W=48U  L=1.6U
M13   5 9 2 2   NT    W=48U  L=1.6U
M14  12 9 2 2   nT  W=48U  L=1.6U
M15   11 11 2 2   nT  W=48U  L=1.6U
M16   6 11 2 2   NT  W=48U  L=1.6U
M17  12 12 1 1   pT  W=37.2U  L=1.2U
M18   6 12 1 1    PT  W=37.2U  L=1.2U
M19   9 9 2 2    NT  W=48U  L=1.6U

.MODEL NT   NMOS (LEVEL=3 TOX=7.9E-9 NSUB=1E17
+ GAMMA=0.5827871 PHI=0.7 VTO=0.5445549 DELTA=0
+ UO=436.256147 ETA=0 THETA=0.1749684 KP=2.055786E-4
+ VMAX=8.309444E4 KAPPA=0.2574081 RSH=0.0559398
+ NFS=1E12 TPG=1 XJ=3E-7 LD=3.162278E-11 WD=7.04672E-8
+ CGDO=2.82E-10 CGSO=2.82E-10 CGBO=1E-10 CJ=1E-3
+ PB=0.9758533 MJ=0.3448504 CJSW=3.777852E-10
+ MJSW=0.3508721)

.MODEL PT PMOS (LEVEL =3 TOX = 7.9E-9 NSUB=1E17
```

```
+ GAMMA=0.4083894 PHI=0.7 VTO=-0.7140674 DELTA=0
+ UO=212.2319801 ETA=9.999762E-4 THETA=0.2020774
+ KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5
+ RSH=30.0712458 NFS=1E12 TPG=-1 XJ=2E-7 LD=5.000001E-13
+ WD=1.249872E-7 CGDO=3.09E-10 CGSO=3.09E-10
+ CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 MJ=0.5
+ CJSW=4.813504E-10 MJSW=0.5)
.ENDS DVCC

.AC DEC 10 10 1000000khz
.PROBE
.END
```

PROGRAM 3

```
x1 1 8 3 0 5 dvcc
x2 3 6 7 8 9 dvcc
x3 8 0 10 6 11 dvcc
v1 1 0 AC 1mV
r1 7 0 1k
r2 10 0 1k
c1 8 0 .001uf
c2 6 0 .001uf
vout1 5 0 dc 0v
vout2 9 0 dc 0v
vout3 11 0 dc 0v

.SUBCKT DVCC 3  4 16 5 6
VDD 1 0 DC 2.5V
VSS 0 2 DC 2.5V
IB 1 12 DC 200uA
M1   17  4  19  2  NT  W=24U  L=0.35U
M2   7   0  19  2  NT  W=24U  L=0.35U
M3   17 16  8   2  NT  W=24U  L=0.35U
M4   7   3  8   2  NT  W=24U  L=0.35U
M5   17  7  1   1  PT  W=15U  L=1.5U
M6   7  17  1   1  PT  W=15U  L=1.5U
M7   12 12  2   2  NT  W=10U  L=1.5U
M8   19 12  2   2  NT  W=10U  L=1.5U
M9   8  12  2   2  NT  W=10U  L=1.5U
M10  16  7  1   1  PT  W=15U  L=1.5U
M11  16 12  2   2  NT  W=10U  L=1.5U
M12  5   7  1   1  PT  W=15U  L=1.5U
M13  5  12  2   2  NT  W=10U  L=1.5U
M14  14  7  1   1  PT  W=15U  L=1.5U
M15  9   9  1   1  PT  W=15U  L=1.5U
M16  9  12  2   2  NT  W=10U  L=1.5U
M17  14 14  2   2  NT  W=10U  L=1.5U
M18  6   9  1   1  PT  W=15U  L=1.5U
M19  6  14  2   2  NT  W=10U  L=1.5U

.MODEL NT  NMOS (LEVEL=2 TOX=7.9E-9 NSUB=1E17
+ GAMMA=0.5827871 PHI=0.7 VTO=0.5445549 DELTA=0
+ UO=436.256147 ETA=0 THETA=0.1749684 KP=2.055786E-4
+ VMAX=8.309444E4 KAPPA=0.2574081 RSH=0.0559398
+ NFS=1E12 TPG=1 XJ=3E-7 LD=3.162278E-11 WD=7.04672E-8
+ CGDO=2.82E-10 CGSO=2.82E-10 CGBO=1E-10 CJ=1E-3
+ PB=0.9758533 MJ=0.3448504 CJSW=3.777852E-10
+ MJSW=0.3508721)
```

```
.MODEL PT PMOS (LEVEL =2 TOX = 7.9E-9 NSUB=1E17
+ GAMMA=0.4083894 PHI=0.7 VTO=-0.7140674 DELTA=0
+ UO=212.2319801 ETA=9.999762E-4 THETA=0.2020774
+ KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5
+ RSH=30.0712458 NFS=1E12 TPG=-1 XJ=2E-7 LD=5.000001E-13
+ WD=1.249872E-7 CGDO=3.09E-10 CGSO=3.09E-10
+ CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 MJ=0.5
+ CJSW=4.813504E-10 MJSW=0.5)
.ENDS DVCC

.AC DEC 10 1K 1000000000khz
.PROBE
.END
```