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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST – 3 EXAMINATION, MAY – 2019

B. TECH. IV SEMESTER (BT)

COURSE CODE: 15B11EC411 **MAX. MARKS: 35**

COURSE NAME: BASIC ELECTRONICS

COURSE CREDITS: 04 **MAX. TIME: 2Hrs**

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

Marks

Q1. (a) Find the nodal voltages of the circuit shown in Fig.1(a). [CO-1] **3**

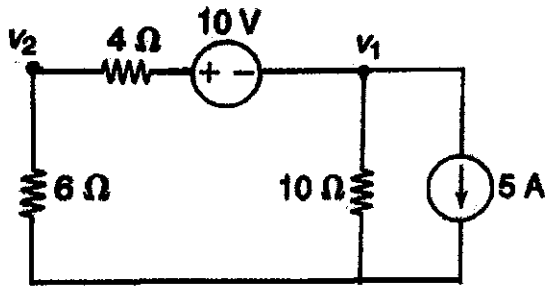

Fig. 1(a)

(b) If V_1=10 V, V_2 = 15V, R_1= 4Ω, and R_2=6 Ω in the circuit shown in Fig.1(b) **2**
Find the Thevenin equivalent for the network to the left of terminals a,b.[CO-1]

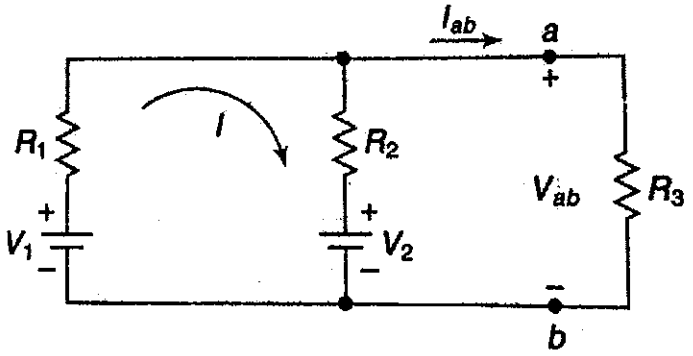

Fig. 1(b)

Q2. (a) In the circuit shown in fig. 2 (a), a silicon diode with knee voltage 0.7 V is used. **3**
The dynamic resistance of the diode in forward bias may assumed to be zero. [CO-2]

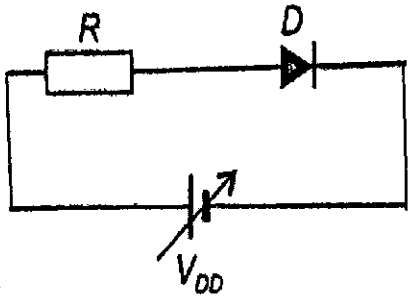

Fig. 2(a)

(i) If V_{DD} = 5 V, what should be the value of R to established a current of 5mA in the Circuit?

(ii) Determine the power dissipated in the resistance R and in the diode D, when a current of 5 mA flows in the circuit at V_{DD} = 6V.

(b) The current flowing in a PN junction diode at room temperature is 200nA, when a large reverse bias is applied. Calculate the current through the diode when 0.1V forward bias is applied. [CO-2] **2**

Q3. (a) Draw a typical common base output characteristics of a pnp transistor and indicate cutoff, active & saturation regions.[CO-3] **2**

(b) For a certain BJT, β=50, I_{CEO}=3μA, and I_C= 1.2mA. Find I_B & I_E. [CO-3] **2**

(c) The d.c. alpha of the transistor in the circuit of fig. 3(c) is 0.96. The voltage drop across 2kΩ is 4V. Determine the base current. [CO-3] **2**

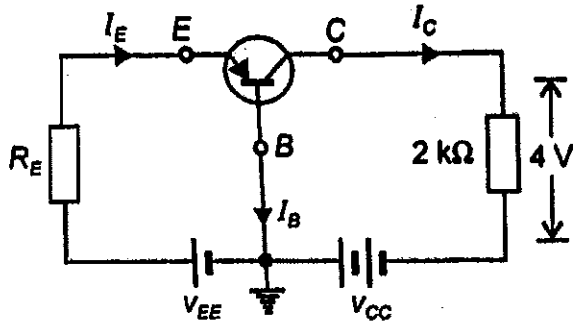

Fig. 3(c)

Q4. (a) Draw a self bias circuit and explain quantitatively why such a circuit is an improvement on the fix bias circuit as far as stability is concerned. [CO-4] **2**

(b) Find the analytical expression for the stabilization factor S for self bias. [CO-4] **2**

(c) In the voltage divider circuit of fig. 4(c), an npn germanium transistor with β =100 is used. Calculate the coordinates of the point Q(V_{CE}, I_C). [CO-4] **2**

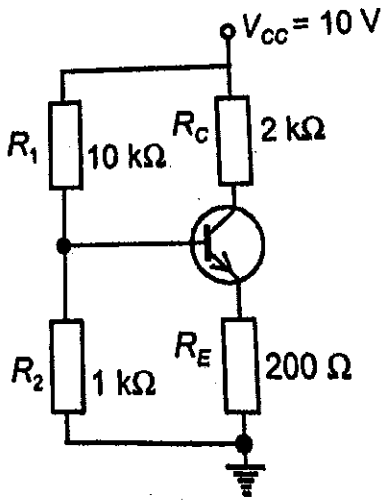

Fig. 4(c)

Q5. (a) Draw a family of common source (CS) drain characteristics of an n-channel JFET and explain the shape of these curves. Indicate ohmic region, saturation region and locus of pinch of region using drain characteristics.[CO-4] **2**

(b) Explain shorthand method for plotting the transfer curve using Shockley equation. [CO-4] **1**

(c) Sketch the transfer curve defined by I_{DSS} =12V & V_P = - 4V. [CO-4] **2**

(d) Given I_{DSS} = 8mA, V_{GS} = -1V & V_P = -4V, calculate drain current I_D. [CO-4] **1**

Q6. (a) Define an exclusive OR gate and draw its symbol and logical block diagram. Also give its truth table. [CO-5] **2**

(b) List the laws and theorems of the Boolean Algebra. [CO-5] **2**

(c) Use NAND gates only to construct a logic circuit with output X = A+B · C [CO-5] **1**

(d) Evaluate the Boolean expression [CO-5] **1/2**

$f = \overline{A} \cdot \overline{B} + A \cdot B + \overline{B} + C$ for $A = 1,\ B = 0,\ C = 1$

(e) Evaluate the Boolean expression for [CO-5] **1/2**

$f = A \cdot B \cdot \overline{C} + \overline{A} \cdot B + A \cdot \overline{B}$ for $A = 1,\ B = 0$ and $C = 1$.

(f) Draw explain the logical diagram of a half – adder using XOR gate & realize it with NAND gates only. [CO-5] **1**