JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-2 EXAMINATIONS- October 2022

B. Tech-III Semester (ECE, Minor Degree in ECE)

COURSE CODE (CREDITS): 18B11EC312 (4) MAX. MARKS: 25

COURSE NAME: Digital Electronics and Logic Design

COURSE INSTRUCTOR: Dr. Naveen Jaglan and Dr. Pardeep Garg MAX. TIME: 1.5 Hours

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Note: *All questions are compulsory. CO indicates course outcomes. Marks are indicated against each question in square brackets.*

Q1. Implement a 3-bit magnitude comparator circuit using logic gates. [CO-3; 3 marks]

Q2. Employing full adders draw the logic diagram of a 4-bit binary parallel adder-subtractor (in one circuit only) and explain its working. [CO-3,4; 3 marks]

Q3. What are the applications of Encoders? Design a priority encoder with 4 decimal inputs (W {MSD}, X, Y, Z {LSD}) where W is having the highest priority and Z is having the lowest priority. [CO-3; 3 marks]

Q4. Design a logic circuit with 4 inputs X1, X2, X3, X4 that will produce output '1' only whenever two adjacent input variables are 1s. X1 and X2 are also to be treated as adjacent. Implement the minimized expression using universal gate only. [CO-1,2; 3+1= 4 marks]

Q5. What are the limitations of parallel adders? Explain with suitable logic diagram how a 4-bit look ahead carry adder can be used to overcome the limitations of parallel adders. [CO-1,3; 1+3 = 4 marks]

Q6. Implement the following logics using multiplexer:

(i) AND gate using 4:1 Multiplexer
(ii) NOR gate using 2:1 Multiplexer
(iii) Half Adder using 2:1 Multiplexer [CO-3; 3 marks]

Q7. Implement the following logic function using 4:1 multiplexer:

$F(A, B, C) = \sum m(1,2,3,5,7)$

(i) Using A and B as select lines
(ii) Using A and C as select lines
(iii) Using B and C as select lines [CO-3,4; 3 marks]

Q8. Implement 4-to-16-line decoder using 2-to-4-line decoders. [CO-2,4; 2 marks]