Munish Sood

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST -2 EXAMINATION- OCT 2019
B.Tech III Semester (ECE)

COURSE CODE: 10B11EC401 MAX. MARKS: 25
COURSE NAME: Digital Electronics
COURSE CREDITS: 4 MAX. TIME: 1Hr 30 Min

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

Q1) Design a 1 bit full adder using 4 X 1 multiplexer. **(4)**

Q2) Implement a decimal to BCD encoder using Logic gates and write the truth table. **(4)**

Q3) Design a 16 : 1 MUX using 4:1 MUX. **(4)**

Q4) Design a full subtractor using 3 to 8 line decoder. **(4)**

Q5) Use karnaugh map to minimize the following expression **(3)**

$$\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + AB\bar{C}\bar{D} + \bar{A}\bar{B}CD + A\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + ABC\bar{D} + A\bar{B}C\bar{D}$$

Q6) Implement the following expressions using only NAND gates **(3)**

(i) $X = A + B$ (ii) $X = \overline{AB} + \overline{C}\overline{D}$

Q7) Implement the following expression using only NOR gates **(3)**

(i) $X = \overline{ABC}$ (ii) $X = (A+B)(C+D)$