Dr. Harsh Sohal

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST-2EXAMINATION – Oct, 2019
B.Tech., Vth Semester, ECE

COURSE CODE: 17B11EC511 MAX. MARKS:**25**
COURSE NAME: **LINEAR INTEGRATED CIRCUITS**
COURSE CREDITS: **4** MAX. TIME: **01** Hr.**30**Min

Note:*All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means. Missing data, if any, can be appropriately assumed.*

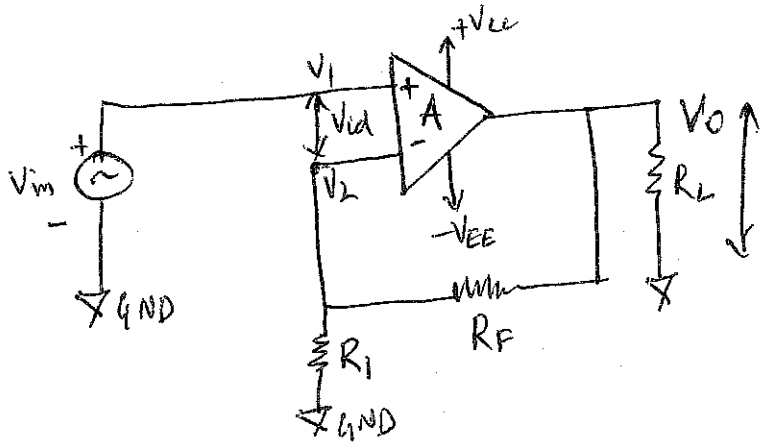
Q1.Answer the following questions briefly and exactly (diagrams may be drawn where required). (1x5)

(a) Give two main reasons why open loop OpAmp configurations are not used in linear applications?
(b) Why negative feedback is desirable in amplifier applications?
(c) In what way voltage follower is a special case of non-inverting Amplifier?
(d) Why is offset minimizing resistor not needed in differential OpAmp circuits?
(e) Define input offset voltage and explain why it exists in all OpAmps?

Q2. (5)

A 741C OpAmp is connected as shown in figure below with R_f=50 kΩ, R_1= 5 kΩ.The OpAmp parameters given are A=500,000 R_i = 5 MΩ Ro = 75 Ω f_o = 5Hz supply voltages = ±15 V Output voltage swing = ±13 V.

Calculate the values of A_F, R_{iF}, R_{oF}, f_F and V_{ooT}.(Symbols used have their usual meaning)

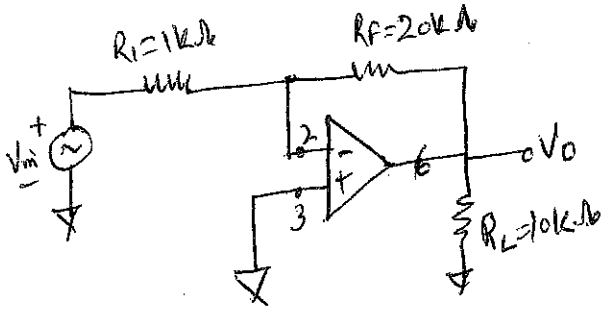


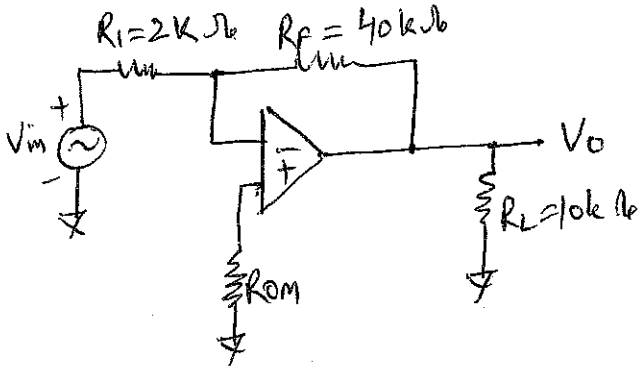
Q3.(3+3+4)

(a) Derive the expression for Offset Minimizing resistor (R_{OM}) for an inverting OpAmp (With required explanation and diagrams).

(b) Compute the maximum possible total output offset voltages in the amplifier circuits shown in Figures below. The OpAmp is MC1536 with following specifications:

V_{io} = 3.5 *mV maximum* I_{io} = *50nA maximum* I_B = *250 nA maximum at* 25^0C

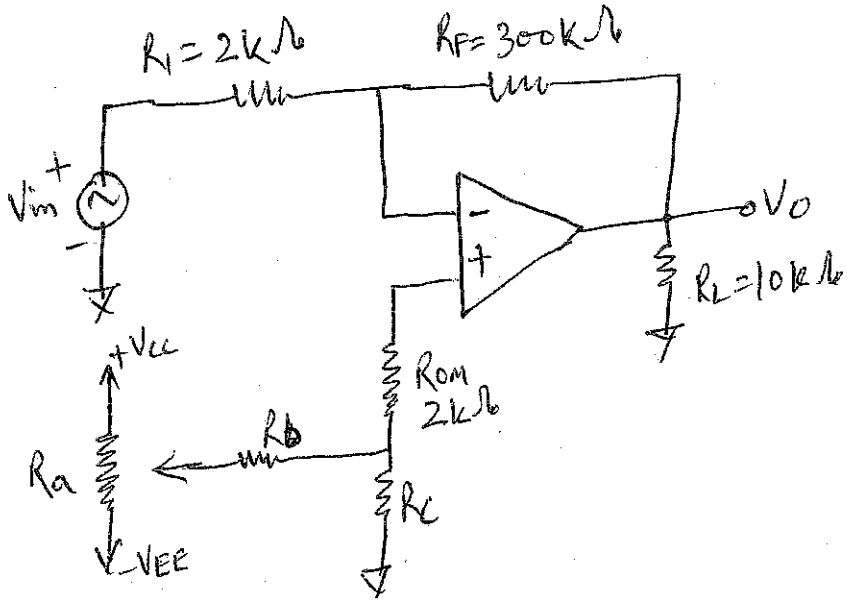




(c) For the figure given below the maximum variation in the poorly regulated supply voltage of ±10V is found to be 2V (maximum). Determine

i) the change in output offset voltage caused by the change in supply voltages

ii) the output voltage V_o if V_{in} = 12 mV dc. The OpAmp is LM307 with SVRR = 96dB



Q4. (3+2)

Derive the expression for f_b(unity gain frequency) and f_a(gain limiting frequency) using the basic and practical integrator circuits. Also*explain* and *draw* a well labelled frequency response of basic and practical integrator circuits.