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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST -2 EXAMINATION- 2019
B.Tech VIII Semester

COURSE CODE: 10B11CI613 MAX. MARKS: 25
COURSE NAME: Computer Organization & Architecture
COURSE CREDITS: 04 MAX. TIME: 1Hr 30 Min

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

[CO4] 1. Let us assume that the processor is going to execute ADD B,A instruction of 16 bit which stores the sum of the contents of memory locations B and A into memory location A. Partial list of opcodes is 0001: Load AC from memory, 0010:Store AC to memory, 0101: Add to AC from memory. PC content is initialized to 300. Memory snapshot is shown as

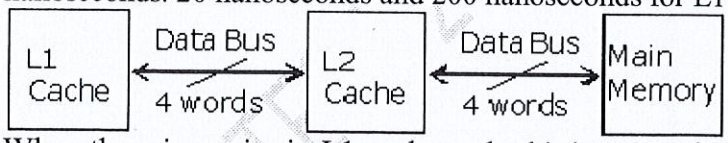
Memory Locations	Instructions (Integer Format)
300	1 9 4 0
301	5 9 4 1
302	2 9 4 1
.....	.....
940	0 0 0 3
941	0 0 0 2

Show step by step execution of the above said instruction using IR, PC, AC and memory locations. [5]

[CO4] 2. (a) Consider a 32-bit microprocessor, with a 16-bit external data bus, driven by an 8-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/s? To increase its performance, would it be better to make its external data bus 32 bits or to double the external clock frequency supplied to the microprocessor? [2.5]

(b) A microprocessor has an increment memory direct instruction, which adds 1 to the value in a memory location. The instruction has five stages: fetch opcode (four bus clock cycles), fetch operand address (three cycles), fetch operand (three cycles), add 1 to operand (three cycles), and store operand (three cycles).
By what amount (in percent) will the duration of the instruction increase if we have to insert two bus wait states in each memory read and memory write operation? [2.5]

[CO3] 3. A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds. 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively.



When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer? [5]

[CO4] 4. Design traditional bus architecture for your computer. Show all components that you can connect within your bus design. What problems you observe in your design as far as contemporary computers are concerned? Modify your design so as it can fulfill the needs of contemporary computers. [5]

[CO3] 5. Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size. **a.** Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag. **b.** Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag. **c.** Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag. [5]