JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION-2022

B.Tech-V Semester (CS/IT)

COURSE CODE (CREDITS): 18B11CI514 (3) MAX. MARKS: 35

COURSE NAME: Computer Organization & Architecture

COURSE INSTRUCTORS: Dr. Vivek, Dr. Pardeep, Sh. Praveen, Dr. Pankaj & Dr. Vipul

MAX. TIME: 2 Hours

Note: All questions are compulsory. Marks are indicated against each question in square brackets.

Q1. **a.** A processor X1 operating at **2 GHz** has a standard 5-stage RISC instruction pipeline having a base CPI (cycles per instruction) of one without any pipeline hazards. For a given program P that has **30%** branch instructions, control hazards incur **2 cycles** stall for every branch. A new version of the processor X2 operating at same clock frequency has an additional branch predictor unit (BPU) that completely eliminates stalls for correctly predicted branches. There is neither any savings nor any additional stalls for wrong predictions. There are no structural hazards and data hazards for X1 and X2. If the BPU has a prediction accuracy of **80%**, calculate the speed up obtained by X2 over X1 in executing P. [4] CO[5]

b. Derive the expression for speedup in pipelining. [2] CO[5]

c. What do you mean by operand forwarding and how will you use it to handle **RAW** (read after write) hazard? [3] CO[6]

Q2. **a.** Consider the following representation of a number in IEEE 754 single-precision floating point format with a bias of **127**. **S=1, E=10000001 and F=11110000000000000000000** Here, S, E and F denote the sign, exponent, and fraction components of the floating point representation. Find out the decimal value corresponding to the above representation. [3] CO[2]

b. Given the following binary number in 32 bit (single precision) IEEE-754 format: **00111110011011010000000000000000**. Find out the decimal value closest to this floating-point number. [3] CO[2]

Q3. **a.** Consider a set-associative cache of size **2KB** with cache block size of **64 bytes**. Assume that the cache is byte-addressable and a **32 -bit** address is used for accessing the cache. If the width of the tag field is **22 bits**, find out the associativity of the cache. [3] CO[3]

b. Consider a system which supports 2-address, 1-address and 0-address **[P.T.O]**

instructions. The system has **'i'** bits instructions and **'a'** bits addresses. If there are **'x'** 2-address instructions and **'y'** 1-address instructions then find out the maximum number of **0-address** instructions supported by the system? [3] CO[1]

c. A **32 – bit** wide main memory unit with a capacity of **1 GB** is built using **256M X 4-bit** DRAM chips. The number of rows of memory cells in the DRAM chip is 2^{10}. The time taken to perform one refresh operation is **80 nanoseconds**. The refresh period is **5 milliseconds**. Find out the percentage of the time available for performing the memory read/write operations in the main memory unit. [3] CO[4]

Q4. **a.** Draw the block diagram of DMA (direct memory access) and write down the steps needed to transfer the data from an I/O device to memory, using DMA. [4] CO[4]

b. What do you mean by memory interleaving? Explain it with the help of an example. [3] CO[3]

Q5. **a.** How many clock cycles are needed to fetch an instruction from the memory? Also write down the micro operations needed to implement it. [2] CO[4]

b. Given a **2048 X 16** memory element. What is the size of the address register, data register, accumulator and system bus? [2] CO[4]