JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION-2022

B.Tech-III Semester (~~CS/IT~~/ECE/~~Civil/BT~~)

COURSE CODE (CREDITS): 20B11EM312 (3) MAX. MARKS: 35

COURSE NAME: DIGITAL ELECTRONICS

COURSE INSTRUCTORS: Dr. Harsh Sohal MAX. TIME: 2 Hours

Note: All questions are compulsory. Marks are indicated against each question in square brackets.

Q1. [CO1, CO2, CO3] [10]

(a) Given X= (11000011)2 and Y = (10101001)2, i) find X+Y ii) find X-Y using 2's complement iii) find X-Y using 1's complement. (Explain the steps) [3]

(b) Reduce the following Boolean expression to a minimum number of literals using Boolean algebra postulates and theorems. [2]

i) (CD`+B`A)(BC`+DA`) ii) ABC+A`B+ABC`

(c) Design a BCD to Gray Code converter circuit using unused combinations of the code as don't care conditions. Implement the circuit diagram using logic gates. [2]

(d) Derive the expression for a 1 bit Full adder from the truth table. Use this 1 bit full adder to design 2bit Ripple Carry Adder circuit for addition of two 2 bit binary numbers. [3]

Q2. [CO2, CO3] [7]

(a)Implement the following functions using a suitable decoder. [3]

$f_1(A,B,C)=\sum m(0,4,7)+d(2,3)$

$f_2(A, B, C)=\sum m(1,5,6, 7)$

$f_3(A, B, C)=\sum M(1,3,4)$

(b) Design a 4:16 decoder using 3:8 decoders. [2]

(c) Differentiate between combinational circuits and sequential circuits. Can we say combinational circuits can be subset to sequential circuits? Why or why not? [2]

Q3. [CO3, CO4] [8]

(a) Explain the Race condition with respect to SR latch. How is it different from race around condition in JK Latch? [3]

(b) Convert an **SR flipflop to a T flip flop** with the help of state transition table and k map simplification method. Draw the circuit using relevant symbols.[3]

(c) To shift a hexadecimal number A into a 4 flip flop serial shift register, evaluate time if frequency is 5 MHz. [2]

Q4. [CO4] [10]

(a) A MOD-16 ripple counter is holding the binary count 1001. What will the count be after 31 clock pulses? [1]

(b) Design a Mod 6 synchronous up counter using JK flip-flop with the help of state transition table and K map approach. [5]

(c) For the circuit below:

(i) Is it a synchronous or asynchronous circuit explain. [1]

(ii) Draw the well labeled input and output waveforms for the circuit. [3]

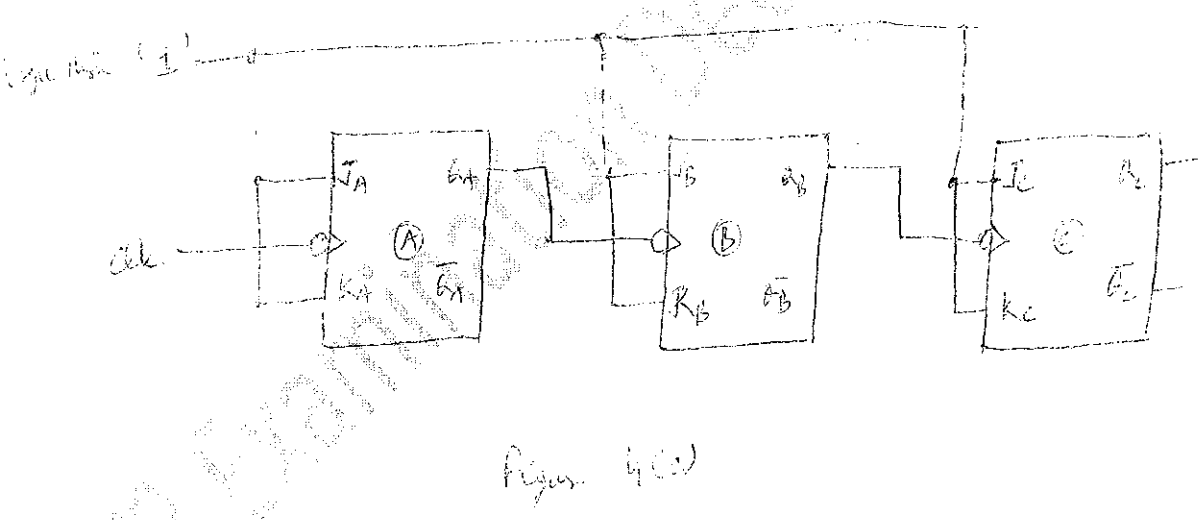

Figure 4(c)