JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATIONS-2022

B.Tech-VII Semester (ECE)

COURSE CODE (CREDITS): 18B1WEC744 (3) MAX. MARKS: 35

COURSE NAME: FPGA BASED INSTRUMENTATION SYSTEM DESIGN

COURSE INSTRUCTORS: Dr. Shruti Jain MAX. TIME: 2 Hours

Note: All questions are compulsory. Marks are indicated against each question in square brackets.

Q1. **1 × 5 = 5** [CO 1, 2, 3, 4, 5]

a. What the code signifies Assign z = c >> 2 ;

b. What is the difference between the following two lines of Verilog Code?

```
#3 a = b;
a = #3 b;
```

c. What gate this equation signifies: assign z = (x & ~y) |(~x & y); Write Verilog code assuming gate level implementation?

d. Why FPGA is Field Programmable Gate Array.

e. "PLA is used to implement sequential logic circuit". Is this statement true/ false? If false state the correct answer.

Q2. a) How many minimum number of AND and OR gates required to Gita for the implementation of Boolean expression using PLA .

$$y1 = f(A,B,C) = \sum m(0,1,3,6,7)$$
$$y2 = f(A,B,C) = \sum m(3,5,6,7)$$

b) Aakash has to implement his final year project on Digital Circuits. He is in opinion of using ASIC and an FPGA design? What is the difference between the two? Which results better? **[2.5 + 2.5]** [CO 2, 4]

Q3. Siya wants to implement Full adder circuit. She has to design the circuit using any two implementation techniques. Help her in designing the circuit on FPGA. Write the code for both techniques. Also, explain the difference between a gate-level implementation and a behavioral implementation of an FPGA design ? **[5]** [CO 3, 4, 5]

Q4 a) For fig 1, write the code for the implementation on FPGA design.

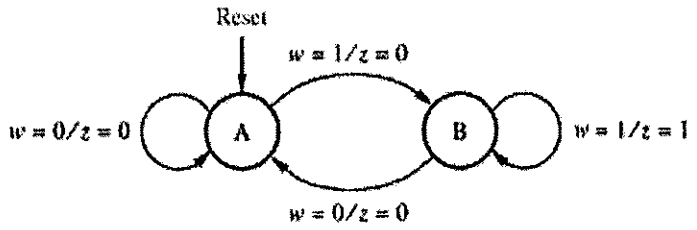

Fig 1

b) Sita is writing code in verilog. She gets confused in the following terms. Help her in explaining the terms.

i. 10
ii. `b10
iii. `h10
iv. 4`b10
v. 8`hfx

[2.5 + 2.5] [CO3, 5]

Q5. Shyam is not able to understand what the role of Switch boxes in FPGA. Explain him in detail.

[5] [CO4, 5]

Q6. Briefly explain every block of the diagram shown in Fig 2. [5] [CO4, 5]

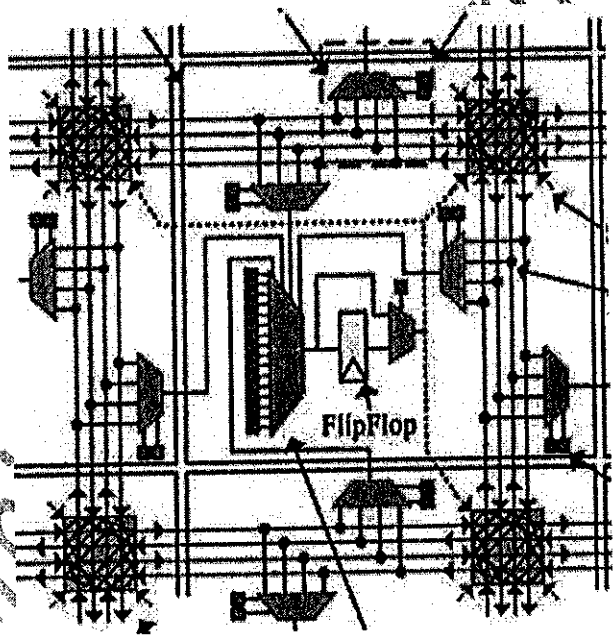

Fig 2

Q7. a) Gita is explaining the concept of reset in class. Explain the significance of Reset. Write a Verilog Code for different types of Reset? State any application where the reset can be used.

b) FPGA as a system on chip platform. Elaborate. [2.5 + 2.5] [CO3, 5]