Dr. Hemraj Saini

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST -II EXAMINATION- February 2018
B.Tech VIth Semester

COURSE CODE: 10B11CI613 MAX. MARKS: 25
COURSE NAME: Computer Organization and Architecture
COURSE CREDITS: 4 MAX. TIME: 1.5 Hr

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

Que.1: ***[4 Marks]*** A cache has 64 KB capacity, 128 byte lines, and is 4-way set associative. The system containing the cache uses 32 bit address.

a. How many lines and sets does the cache have?
b. How many entries are required in the tag array?
c. How many bits of tag are required in each entry in the tag array?
d. If the cache is write-through, how many bits are required for each entry in the tag array, and how much total storage is required for each tag array if an LRU replacement policy is used? What if the cache is write-back?

Que.2 ***[4 Marks]*** Suppose that SRAM costs $25 per MB for an access time of 5ns, DRAM cost $1 per MB with an access time of 60ns, and disk space cost $10 per GB with an access time of 7 ms.

a. For a memory system with 256 KB of virtual memory of cache SRAM, 128 MB of main memory DRAM, and 1 GB of virtual memory (implemented as disk), what is the total cost of the memory system and the cost per byte?
b. If the hit rate at each level in the memory hierarchy is 80 percent (expect the last), what is the average memory access time?
c. What is the average access time if the hit rate at each level except the last is 90 percent?
d. How about if the hit rate is 99 percent at each level except the last?

Que.3 ***[4 Marks]*** A DMA module is transferring characters to memory using cycle stealing, from a device transmitting at 9600 bps. The processor is fetching instructions at the rate of 1 million instructions per second (1 MIPS). By how much will the processor be slowed down due to the DMA activity?

Que.4 ***[3 Marks]*** A 32 KB RAM is formed by 16 numbers of a particular type of SRAM IC. If each needs 14 address bits, determine:
(a) IC capacity
(b) Memory organization
(c) Address rang for each block

Que.5 ***[2x5=10 Marks]*** Answer the following questions-

a. Differentiate between RAID-0 and RAID-3.
b. Explain multiple zones recording over magnetic disk. Why it is better than tradition disk recording?
c. What is split cache? Write its advantages.
d. Provide the comparisons of SDRAM and RDRAM?
e. What is write through cache?