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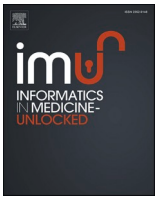

FPGA implementation of collateral and sequence pre-processing modules for low power ECG denoising module

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ABSTRACT

ECG signal recording easily suffers from interferences in the environment, such as patient movement, and position of electrodes. For primary diagnosis, doctors need noise-free ECG signals. This paper presents the hardware implementation of denoising of ECG signals using various types of linear windowing techniques and non-linear discrete wavelet transform (DWT) on the proposed architectures using FPGA. DWT has extensive usage in different image processing applications as image compression and information hiding. The simulation results obtained from various techniques and architectures are compared using MATLAB and XILINX VIVADO EDA tools. The performance evaluation of the proposed methodology is evaluated on the basis of resource utilization and on-chip power consumption on the different FPGA boards (Virtex, Kintex, and Zedboards) using VIVADO. From the simulation results, inference has been drawn that Haar wavelet consumes only 0.76% of LUTs, 5.03% of slice registers and 6.7% of DSPs in comparison with other wavelet and window techniques using Zedboard. The Haar wavelet based pre-processor design only consumes 136 mW of on-chip power. The proposed pre-processing module can be used in wearable and portable biomedical equipments.

1. Introduction

Biomedical signals are the indications of physiological events of an individual, varies from protein sequences, tissue and organ images, to neural and cardiac rhythms. These bioelectric signals vary with the physiological processes in the body, which are acquired by using the electrodes [1]. Every physiological process is related to certain kinds of signals that reflect their events and description. Different types of disorders and diseases can often be detected by monitoring these signals and comparing them to their norms. A one-dimensional time series plot of any signal monitored over a period of time is termed as a physiological signal. The electrical activity produced by the heart radiates in different directions is graphically recorded by the clinicians termed as an electrocardiogram (ECG) [2,3]. Several electrodes are placed on the body to acquire the ECG signal. The diagnosis of cardiovascular diseases employing the ECG signal has emerged as one of the extensively utilized tools in medical practice. ECG signal constitutes mainly five waves that reflect the working of the heart during a cardiac cycle; these waves are termed as: P, Q, R, S and T; the Q, R, and S waves are taken as a single composite wave labelled as the QRS complex.

The ECG signal is easily hampered by various kinds of noises produced while acquiring and recording from a patient's body. There are several kinds of noises found in ECG recording like Power Line Interference (PLI), electrode impedance noise, motion noise, Electromyography (EMG), Base Line Wandering (BLW), etc [4]. The most common and influential noises are EMG, BLW, and PLI. A large deviation in the baseline of the ECG signal arises due to the presence of low-frequency BLW noise; which makes the ECG signal analysis challenging. It arises due to the skin-electrodes improper interference, patient movement, and skin resistance. EMG noise is a high-frequency noise. This type of noise is produced by the electrical activity of muscles other than the heart. The repolarization and depolarization generated due to other muscle contractions in the region of ECG electrodes can also be acquired during ECG recording. To remove these interferences from the ECG signal, denoising of the signal should be done. An efficient denoising technique removes the artifact without influencing the shape of ECG. The applications of ECG have motivated researchers to develop efficient denoising techniques such as FIR filters, fuzzy logic, wavelet transform, empirical mode decomposition, morphological filters, and adaptive filters. A less research has been done on the hardware implementation of FIR filters using Field Programmable Gate Array (FPGA). FPGA is a type of re-programmable integrated circuit besides the digital

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signal processor (DSP) and micro-controller unit (MCU) [5]. The challenges encountered during FPGA utilization for signal processing algorithms are significant. Almost every processor is capable of performing DSP algorithms since they all can perform mathematical operations. The only difference between a general-purpose DSP and an FPGA is how well they perform this function. High performance and energy-efficient implementations of digital systems remain a design challenge, especially in portable devices. This requires optimization at all levels of design hierarchy. At the coarse-grained level, efficient architectures are needed and at the fine-grained level, efficient algorithms can help to reduce the overall power consumption of the system.

Speed is one of the most essential factors that influence computation time, as well as one of the most crucial market factors. The parameters of the filters are adjusted with each iteration, and the error between the input and the intended signal gets reduced with each iteration. The error reaches zero after a certain number of iterations, and the desired signal is obtained. Due to their parallel nature, FPGAs have an edge over DSPs in terms of speed. When compared to DSPs, FPGAs can manage more processes at once, but DSPs can only handle a limited amount of simultaneous instructions at a time. The noise reduction in real time is influenced by the speed of both processors. Unless a high-end DSP processor is employed, a software solution of adaptive noise filtering rarely meets the needed processing speed. A specific hardware implementation employing an FPGA can represent a practical solution. FPGAs are substantially quicker than DSP processors in high-speed applications. When opposed to FPGAs, DSP boards have some disadvantages when it comes to high-speed applications. In addition, FPGA partitioning can provide higher throughputs than DSP processors. DSP is more useful for basic applications, whereas FPGA is more trustworthy for complicated processing such as biological signal processing.

The dynamic power is dissipated only when transistors are switching & leakage power is consumed even if transistors are idle. Therefore, leakage power is proportional to the number of transistors and hence their silicon area [6].

1.1. Literature review

From the past few years, the filtering of the biomedical signals is done using classical digital signal processing techniques. The applications of digital filter design and spectral analysis utilized various types of windowing functions [7]. The FIR filter performance enhancement has been studied by using an adjustable Kaiser Window technique. Also, the implementation of the FIR low-pass filter is done using the Kaiser window during the pre-processing stage is proposed [8]. A simple technique is suggested for the design of the FIR filter except for rectangular window function; also the comparison has been done with another state of art methods [9].

Nowadays, many innovative approaches for the ECG pre-processing stage have emerged. The major research is carried on the wavelet transform (WT) [1]. The Fourier Transform (FT) helps to determine the frequency present in a given signal. But, in case of these non-stationary signals like ECG, FT does not know at what time the frequencies are present. So, to conquer this challenge WT is utilized as it transforms the input signal into another form that signifies the signal in a more valuable form by convolving the input signal with function termed as wavelet [11]. This wavelet function is moved at different locations, squeezed and stretched on the input signal. The wavelet function utilized as a mathematical microscope at different stages of magnification.

A soft threshold-based WT is proposed for the non-stationary environment in which the elimination of some wavelet coefficient is done for obtaining noiseless signal [12]. This research work also expressed the drawbacks of some popular algorithms namely Adaptive Impulse Correlated Filter (ACF), Time Sequence Adaptive Filter (TSAF), Least Mean Square (LMS) adaptive method, Signal Input Adaptive Filter and on a non-stationary signal like ECG. The authors introduced a wiener filter based on WT to eliminate high-frequency noise from the informatory ECG signal by modifying the coefficients of WT depending on the estimated noise level [13]. The wavelet filtering with hybrid thresholding is also investigated been done in the literature for pilot estimation. To eliminate the high-frequency noise in the signal symlet wavelet having order 8 and decomposition level up to 6 is proposed using the wavelet shrinkage method of Empirical Bayes posterior median [14]. A novel approach is introduced to denoise the ECG by adaptive bionic WT termed as Bionic Wavelet Transform (BWT). High sensitivity, non-linearity, and frequency selectivity are some of the advantages of BWT. It also has the ability to reconstruct the signal by inverse transform and concentrated energy distribution. A denoising technique based on DWT is introduced and results are compared with existing methods in terms of SNR. It illustrates that WT provides better results than other techniques [15].

Motivation: As a result, the power unit in the IC expands in size. The demand for low-power devices is increasing as the number of battery-powered complex functioning life-saving devices such as peacemakers and other implantable medical tools grows. Researchers are devoting more effort into developing low-power components and design approaches than they have in the past. In high-power applications, on the other hand, the rate of silicon failure doubles with each increase in temperature. Reduced power consumption is a natural progression that has gained prominence with the advent of deep submicron nodes and nanoscale technologies.

1.2. Research contribution

Accurate diagnosis of any disease from the acquired biomedical signal is very difficult from the sensitive medical monitoring equipment such as ECG machine. ECG signals obtained can be easily corrupted with various mechanical and electrical noises namely EMG, BLW, and PLI, etc. This undesirable interruption in the cardiac signal hampers the ECG signal analysis. Therefore, a noiseless ECG signal is the primary requirement for clinicians to diagnose heart-related problems correctly. Implementation of digital filter algorithms on single-chip, DSP and programmable logic devices are slow, sluggish and non-flexible compared to the FPGA. Implementing them using FPGA has the characteristic of high flexibility, low production cost, real-time, and faster processing speed.

A lot of academicians have proposed numerous filters to eliminate these undesirable signals for ECG denoising algorithms. The output ECG signal obtained from the various linear and non-linear filters would be compared statistically in a noisy environment. This work proposes a methodology to design and implement different architectures to denoise ECG signal using FPGA with different boards (Virtex, Kintex and Zedboard). The higher sampling rate is the advantage of FPGA for designing a digital filter application over DSP chips and it is also cost-efficient than ASIC for moderate volume application. The complexities of the implemented circuit on FPGA, in terms of a number of slice LUTs, slice registers and DSP are evaluated and compared with other state of art techniques.

This research work is structured as Section 2 describes the theory and proposed methodology utilized in this article comprising mainly of three parts: ECG database, ECG pre-processing, proposed filter's architecture illustrated in Fig. 1. The results of proposed pre-processing architecture

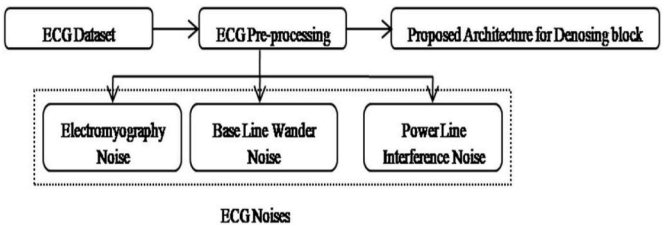

Fig. 1. Methodology of ECG pre-processing block.

using different techniques are discussed in Section 3 along with their RTL schematic, Scope waveforms, resource utilization and power consumption from different types of FPGA board. Section 4 concludes the proposed work including future scope.

2. Theory and methodology

Generally, biomedical signal processing comprises of three stages: Pre-processing, Feature Extraction and0classification stage for the final diagnosis of diseases. In this paper, the authors are emphasizing on the hardware implementation of ECG pre-processing stage to remove unwanted noises from the useful signal using FPGA and help the clinicians for an accurate diagnosis. Fig. 2 signifies the proposed methodology of the implementation of the ECG denoising block using different FPGA blocks. This methodology successfully improves the extracting precision and speed that provides strong stability for the ECG denoising.

2.1. ECG dataset

The input ECG signals are extracted from the standard MIT-BIH Arrhythmia Database normal/abnormal ECG beats based on MIT-BIH database that is considered are classified, such beats are considered to be processed using the denoising block. Each signal0is referenced from the0MIT-BIH database by0selecting the target 0database (MIT-BIH Arrhythmia0Database (MITDB)) that contains the selected records. The records are0digitized at 360 samples0per second per channel with an011-bit resolution0over a 10 mV0range. Those records are fed to the denoising block to start the processing of the acquired0ECG signals.

2.2. ECG pre-processing

ECG signals suffer from two main types of noise: Low-frequency noise represented as BLW and High-frequency noise such as EMG and PLI. The valuable information in the ECG signal lies in between the frequency range from 0.5 Hz to 100 Hz. Pre-processing is done by employing linear and non-linear filters to diminish these undesirable signals. In this paper, several types of windowing techniques and wavelet transforms are utilized due to its simplicity in FPGA implementation. To perform the pre-processing step the authors have divided this phase into two parts: selection of the coefficients and filter's architecture.

2.3. Selection of coefficients

The numbers of filter coefficients are computed based on various windows and wavelet functions. In this work, the authors have considered four types of the window as well as wavelet functions. These functions incorporate Kaiser, Blackman, Bartlett, and Hamming as window functions and Haar, Coiflet, Daubechies and biorthogonal as wavelet functions [16].

The output of the system is computed on the basis of the order of the filter and filter's coefficients. Filter designing for a specific application such as low pass and high mainly depends on the value of filter's coefficients which can be easily calculated by employing tools from the MATLAB [17]. In this article, the authors have taken the entire conventional window and wavelet filtering techniques. Further, different combinations of these designs are considered to meet the specification of low resource utilization and power on FPGA. The filter specifications to eliminate the undesirable ECG noises are as following:

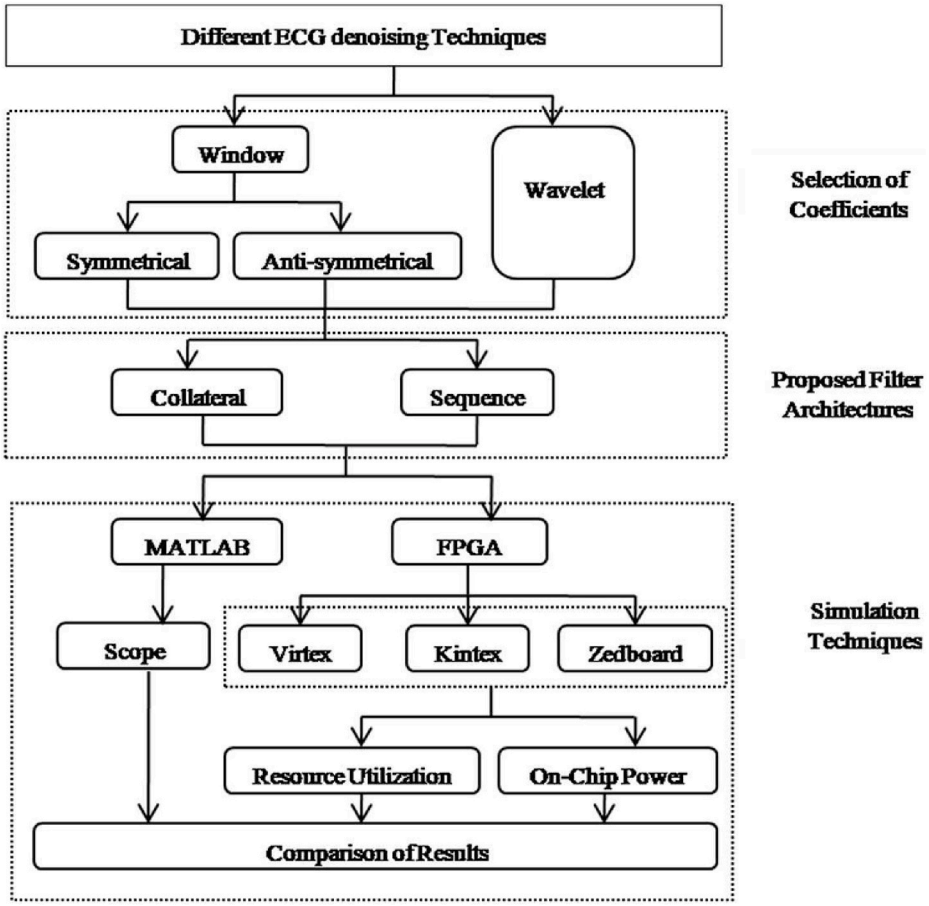

Fig. 2. Proposed methodology for ECG denoising block.

The order of the filter (M): **7**.
High Pass Filter Cut-off Frequency (ω_c): **0.5 Hz**.
Low Pass Filter ω_c: **100 Hz**.
The FIR digital filter equation for window function is:

$$y(n) = x(n)*h(n) \tag{1}$$

$$y(n) = \sum_{k=0}^{M-1} h(k)x(n-k) \tag{2}$$

y(n): Output Response of the Filter
x(n): Input Response of the Filter
h(n): Impulse Response of the filter.
The general mathematical analysis of the ideal frequency response is illustrated in Table 1.

2.3.1. Windows coefficients

Window techniques are commonly used for digital filter design such as Finite duration unit pulse response (FIR) filter. The FIR filter design is popularly used nowadays for the measurement and noiseless ECG signal [6]. These filters are utilized to remove the noisy signal from the valuable biomedical signal and its consequence is observed on the input signal that can be defined in the time domain. But, only the time domain technique of ECG signal analysis is not enough to study all the prominent features. Therefore, the filters are also designed in the frequency domain to illustrate the signal in terms of frequency [3]. There are two different types of core architectures that are used for denoising ECG signals for windowing functions namely anti-symmetric and symmetric. Adder, Multiplier and delay units are the basic structures of the core architecture and it is observed that symmetrical structures utilize less power and resources as compared to anti-symmetric structure due to the presence of symmetrical coefficients.

2.3.2. Wavelet coefficients

There are different types of analysis. The time-domain analysis is carried out by Shannon Nyquist Theorem, frequency analysis is analyzed by Fourier Transform, Short-Time Fourier Transform is analyzed by Gabor Wavelet and the last is Wavelet Transform. In this paper, analysis has been done by using Wavelet transform. There is a difference between Fourier analysis and wavelet transform. Fourier analysis involves the splitting of any signal into sinusoidal waves of different frequencies while wavelet transforms consist of the splitting of a signal into a shifted and scaled version of the original wavelet which is known as mother wavelet. DWT is utilized to analyze the ECG signal to a range of different frequencies. Often the signals of ECG are unstable because they determined by the subject condition. In this research, various wavelet coefficients namely Daubechies, Coiflet, haar and biorthogonal are used. The prominent application of DWT is the removal of unwanted frequency from a noisy signal. The expansion of the wavelet in every ECG signal is expressed by Eq. (3):

$$(x) = \sum_{k} c_{j0}(K)\varphi_{j0,k}\,(x) + \sum_{j=j0}^{\infty}\sum_{k} dj\,(k)\psi_{j,k}(x) \tag{3}$$

Where, $(x) \in L2\ (R)$, 2 (R): relative to the wavelet (x), and c_{j0} are the estimation coefficients. In the first sum, the estimation coefficients c_{j0} is represented as the result of the interior product process in the original signal (x).

Table 1
Ideal Frequency response of various filters.

Type of Filter	Type of Noise Removal	Frequency Response h [n]
High Pass Filter	Base Line Wander	$h[n] = \frac{\sin[\omega_c(n-M)]}{\pi(n-M)};\ n \neq M$ $\omega_c/\pi; n = M$
Low Pass Filter	Electromyography	$h[n] = \frac{\sin[\omega_c(n-M)]}{\pi(n-M)};\ n = M$ $1 - \left(\omega_c/\pi\right); n \neq M$
M: Order of the filter		ω_c: Cut-off frequency

2.4. Proposed Filter's architecture

Digital filters shall be designed in MATLAB to denoise the ECG signal with muscular noise and the performance will be evaluated based on speed, power, and area. Further, the filters with the desired specifications are designed using Verilog Hardware Description Language (HDL). Simulation of the architectures has done using VIVADO 2018 simulator for verifying the functionality of these designs and the architecture is implemented on Xilinx Spartan 6 FPGA. The proposed FPGA based low-cost ECG system operates with high reliability, better performance, and low maintenance. The algorithm will analyze the composition of the ECG signals to retain clinical information. In this paper, authors have proposed two types of architecture for ECG denoising: collateral and sequence as illustrated in Fig. 3 and Fig. 4. The proposed architectures include three types of filter particularly high pass filter (HPF), low pass filter (LPF) and notch filter to eliminate EMG, BLW, and PLI respectively. The core structure of the proposed architecture is composed of anti-symmetric and symmetric design. The scope block is used to observe the signal in time-domain analysis.

Communication energy dominates computations, whether the communication is moving data in and out of memories or moving data over wires to different processing points on the chip. Tuning the level of parallelism exploited for an application can shift this communication energy between memories and interconnection required for the computation. As a result, for each application and dataset size, there is an optimal level of parallelism that minimizes the energy. The optimal level of parallelism grows with problem size, as does the energy benefit compared to a nonparallel design.

3. Results and discussion

The hardware implementation of digital circuits is required because accelerates the execution speed from hours to several minutes or seconds. However, to achieve high speed and real-time execution, hardware design needs to be concentrate since the resources as logical components and frequency are limited. To apply digital circuits on hardware, different technologies had been used as application-specific integrated circuits (ASIC) and field-programmable gate arrays (FPGAs). Cost reduction played a major role in the widespread use of FPGAs since there was a reduction of 100% in the cost of building blocks from 1990 to 2003. At the same time, the continuous increase in the cost of ASICs compared to advances in semiconductor manufacturing made the FPGA a better alternative for embedded systems, as the cost of making incremental changes to FPGA designs is negligible when compared to the large expenses involved in the re-manufacturing of ASICs. FPGA is also considered as one a successful technology for developing systems for real-time operation. It has a parallel execution nature where several processes can be executed concurrently which produces the real-time response.

The proposed work deals with two types of software tools: MATLAB and VIVADO. To obtain the resource utilization and power consumption on different FPGA Boards, the authors have employed VIVADO tool from XILINX software. The selection of an appropriate tool for hardware designing is a very crucial step as it affects the development time, power consumption and cost of the research work. Initially, Hardware Description Language (HDL), such as Verilog or VHDL as structural or behavioral specifications are targeted for the hardware netlist generation for FPGA. From the past few years, the focus has been shifted towards higher-level languages than traditional HDLs. Various systems help in the design, modeling, and simulation of the systems. Though, all these systems are still under development and have their limitations. The XSG is a DSP design tool from Xilinx that enables the use of the

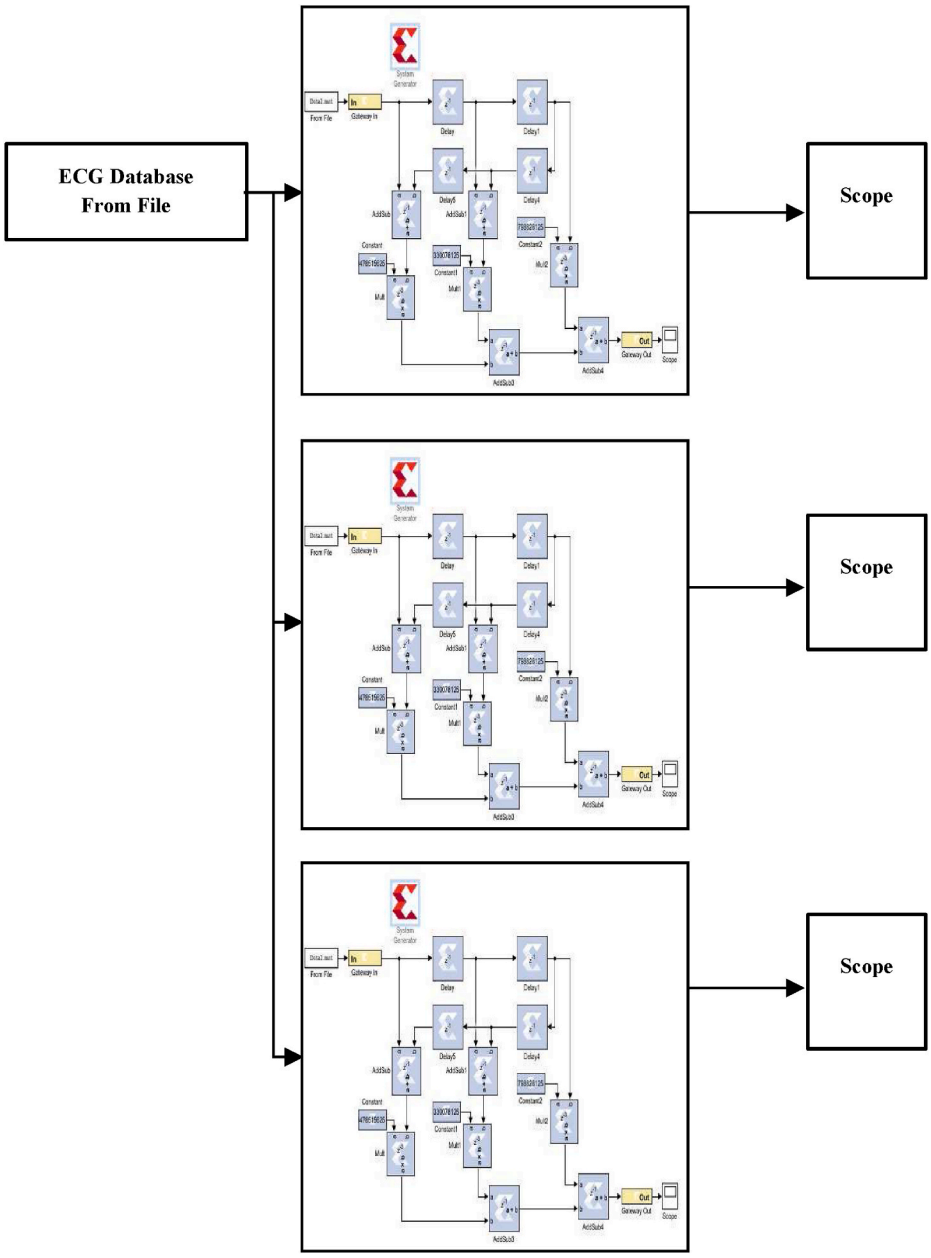

Fig. 3. Collateral ECG Denoising block.

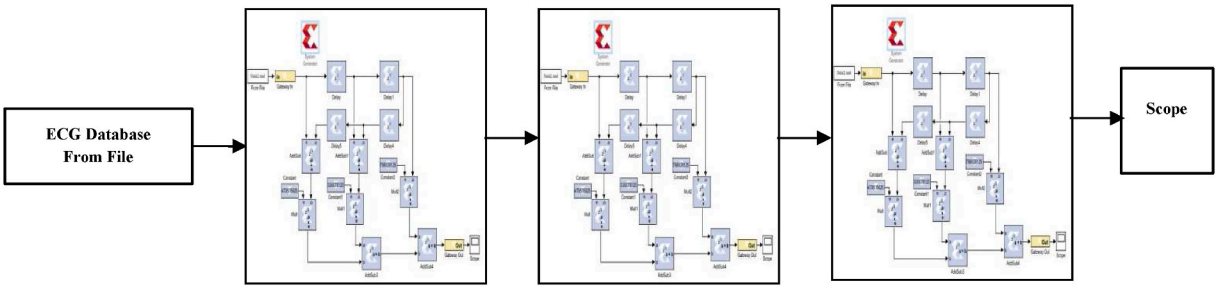

Fig. 4. Sequence ECG Denoising block.

Mathworks model-based design environment Simulink for FPGA design [17,18]. Fig. 5 demonstrates the link between Matlab and Vivado and the functioning of Xilinx system generator.

Designing DSP algorithms on FPGAs is a quite challenging task. The natural path of DSP algorithms is to use software based languages such as C and implement the algorithms on DSP processors. FPGAs use hardware description language (HDL) to do the same task. The conversion of a software based algorithm to hardware is an automated

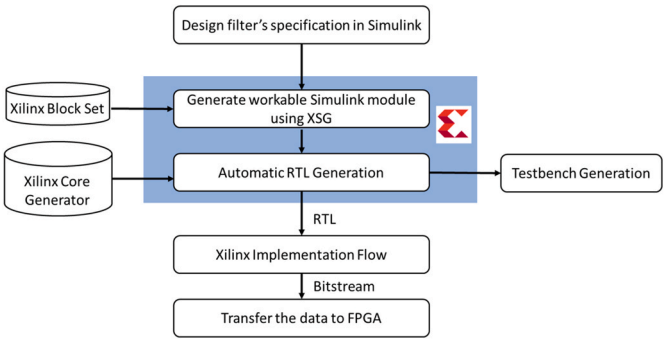

Fig. 5. FPGA/DSP design flow.

process most of the time. However, the DSP algorithms could be designed in HDL from the beginning with special expertise. Fig. 5 shows the DSP design flow on FPGAs using several tools offered by Xilinx. A MATLAB algorithm can be converted to registered transfer level (RTL) using AccelDSP design tools or it can be combined with Simulink blocks. Xilinx provides a DSP library to implement complex DSP algorithms such as filters that can be used in any design. Also, Xilinx coregen tool can be used to create complex DSP functions in RTL. Coregen is a parameterized tool that can generate complex functions. A Simulink design can be converted to RTL automatically using System generator tool. In any case, an RTL based design can be created that can be placed and routed using Xilinx ISE tool set. This can create the bitstream needed to configure the FPGA.

It also delivers a system integration platform for the design and implementation of DSP FPGAs that allows the RTL, Simulink and MATLAB components of a DSP system to come together in a single simulation and implementation environment. This research work deals with two types of tools: XSG and XILINX VIVADO [18]. To obtain XSG results, System Generator 2018.1 is used from the Simulink model using the scope. While the XILINX based results are acquired on Zedboard ZYNQ-7000 AP-SoC using the VIVADO tool. The hardware implementation environment results are divided into two parts:

1. Collateral ECG denoising
2. Sequence ECG denoising

In this section, an efficient method of implementing FIR filters is presented. This method uses the FPGA resources efficiently and optimizes the FPGA for area and performance. This discussion continues with addressing the leakage power consumption for on-chip memory that is an important factor in determining the ECG input of the total power. The range of DSP functions that can be implemented on FPGAs is enormous. Among all DSP functions, FIR filters are common in signal processing applications.

This paper has presented an initial work of the authors in their attempt to architect a flexible platform for ECG analysis. Whereas the technologies available for the realization of this architecture are very mature, identification of the interfaces in this architecture along with their definitions need be done very carefully to, fully, ensure extensibility of the ECG analysis, which can be scheduled on this architecture. Simultaneously, it is essential that the architecture shall be extensible by itself. The identification of the interfaces and their definitions is the ongoing activity of the authors. The authors wish to model this architecture, realize this architecture and conduct case studies on this architecture as their future research work.

3.1. MATLAB implementation

MIT/BIH taken from online platform has already been contaminated with EMG, BLW and PLI. The simulation is carried on SIMULINK in which Fig. 6(a) illustrate Raw ECG signal of record number '100' having

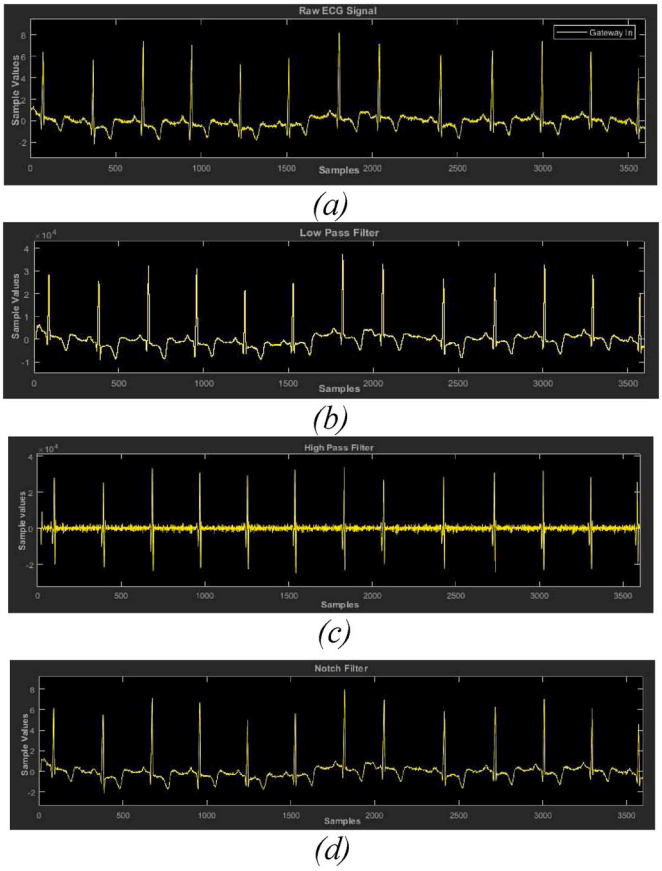

Fig. 6. Scope results (a) Input ECG signal (b) Electromyography Noise Removal (c) Base Line Wander Removal (d) Power Line Interference Removal.

3600 samples with a time length of 10 s. Fig. 6(b) shows the removal of the high-frequency noise by applying low pass filter having 'fc' 100 Hz. Fig. 6(c) shows the output of high pass filter having cut-off frequency 'fc' 0.5 Hz to remove BLW noise from the input. Fig. 6(d) uses the notch filter with 'fc' of 49.5 and 50.5 Hz to eliminate PLI from the useful informatory signal.

3.2. VIVADO implementation

Zedboard from XILINX Zynq-7000 family is selected for XSG flow and Verilog language is utilized for the netlist generation. The authors have taken the FPGA clock period as 10 ns. The whole analysis is performed post-synthesis through which resource utilization and power consumption are calculated. Table 2 and Table 3 signifies the utilization of basic units (Slice LUT, Slice register, DSP) for proposed collateral and sequence architectures of ECG denoising block. It also incorporates the anti-symmetric and symmetric for windows and wavelet function architectures of the core structure. For simulation, the authors have considered three types of FPGA board: Virtex, Kintex and Zedboard and compared their resource utilization and on-chip power for the proposed architectures.

The three different boards were used for the simulations on the proposed architectures using windows (anti-symmetrical & symmetrical) and wavelet techniques. The proposed methodology performance is evaluated based on resource utilization and on-chip power consumption on the different FPGA boards using VIVADO. The inference has been drawn that our proposed Collateral architecture yields minimum on chip power 0.142 W and 0.139 W when using anti-symmetric and symmetric window technique for Bartlett window, and 0.262 W when using wavelet technique for Harr window.

From the Table 2, it is inferred that out of the three boards, Zed board

Table 2
Resource utilization and On-Chip power of Collateral denoising block.

Filter Architecture			Virtex Board (XC7V585T)				Kintex Board (XC7K70T)				Zedboard (XC7Z007S)			
			Resource Utilization			On-Chip Power (W)	Resource Utilization			On-Chip Power (W)	Resource Utilization			On-Chip Power (W)
			Slice LUT	Slice Registers	DSP	Total	Slice LUT	Slice Registers	DSP	Total	Slice LUT	Slice Registers	DSP	Total
Windows	Anti-symmetric	Kaiser	621	1149	30	2.076	621	1149	30	0.774	621	1149	30	0.310
		Bartlett	621	1149	30	2.074	621	1149	30	0.772	621	1149	30	**0.142**
		Blackmann	621	1149	30	2.066	621	1149	30	0.761	621	1149	30	0.292
		Hamming	621	1149	30	2.075	621	1149	30	0.772	621	1149	30	0.307
	Symmetric	Kaiser	462	894	18	2.073	462	894	18	0.763	462	894	18	0.299
		Bartlett	462	894	18	2.071	462	894	18	0.772	462	894	18	**0.139**
		Blackmann	462	894	18	2.060	462	894	18	0.770	462	894	18	0.288
		Hamming	462	894	18	2.070	462	894	18	0.761	462	894	18	0.296
Wavelet		Haar	309	597	18	2.041	309	597	18	0.728	309	597	18	**0.262**
		Daubechies	729	1337	34	2.082	729	1337	34	0.781	729	1337	34	0.316
		Coiflets	729	1337	34	2.079	729	1337	34	0.777	729	1337	34	0.313
		Biorthogonal	729	1337	34	2.073	729	1337	34	0.770	729	1337	34	0.301

Table 3
Resource utilization and On-Chip power of sequence denoising block.

Filter Architecture			Virtex Board (XC7V585T)				Kintex Board (XC7K70T)				Zedboard (XC7Z007S)			
			Resource Utilization			On-Chip Power (W)	Resource Utilization			On-Chip Power (W)	Resource Utilization			On-Chip Power (W)
			Slice LUT	Slice Registers	DSP	Total	Slice LUT	Slice Registers	DSP	Total	Slice LUT	Slice Registers	DSP	Total
Windows	Anti-symmetric	Kaiser	621	1149	30	2.076	621	1149	30	0.774	621	1149	30	0.299
		Bartlett	621	1149	30	2.074	621	1149	30	0.772	621	1149	30	**0.138**
		Blackmann	621	1149	30	2.066	621	1149	30	0.761	621	1149	30	0.292
		Hamming	621	1149	30	2.075	621	1149	30	0.772	621	1149	30	0.307
	Symmetric	Kaiser	462	894	18	2.067	462	894	18	0.762	462	894	18	0.289
		Bartlett	462	894	18	2.074	462	894	18	0.770	462	894	18	**0.136**
		Blackmann	462	894	18	2.072	462	894	18	0.758	462	894	18	0.281
		Hamming	462	894	18	2.060	462	894	18	0.769	462	894	18	0.295
Wavelet		Haar	309	597	18	2.041	309	597	18	0.729	309	597	18	**0.260**
		Daubechies	729	1337	34	2.082	729	1337	34	0.785	729	1337	34	0.312
		Coiflets	729	1337	34	2.086	729	1337	34	0.779	729	1337	34	0.310
		Biorthogonal	729	1337	34	2.090	729	1337	34	0.781	729	1337	34	0.307

yields the minimum on chip power and uses less resource elements. ZedBoard is a low-cost development board for the Xilinx Zynq-7000 programmable SoC (AP SoC) in comparison with other two boards. There are several expansion connectors that expose the programmable logic I/Os and processing system for easy user access. Zedboard can be used in Linux/Android/RTOS development, general Zynq-7000 SoC prototyping video processing, software acceleration, and embedded ARM processing.

The inference has been drawn that our proposed Sequence architecture yields minimum on chip power of 0.138 W and 0.136 W when using anti-symmetric and symmetric window technique for Bartlett window, and 0.260 W when using wavelet technique for Haar window. From the table it is inferred that out of the three boards, Zedboard acquire the minimum power consumption also it works without importing off-shelf components which make the proposed design applicable to a wide range of devices. The minimum resource utilization for both the proposed architectures are attained from the symmetrical architecture of windows technique as it acquires only 0.76% LUTs, 5.03% slice registers and 6.7% of DSP units. Figs. 7 and 8 illustrates the RTL schematic of the collateral and sequence ECG denoising architecture respectively for the elimination of unwanted signal present in the ECG. Fig. 8 also signifies the inclusion of basic components for the designing of these digital filters for its core structure.

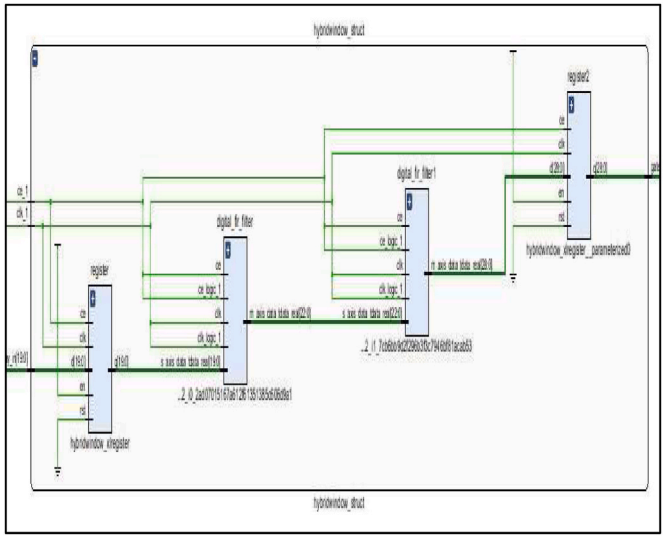

Fig. 7. RTL schematic of Collateral architecture.

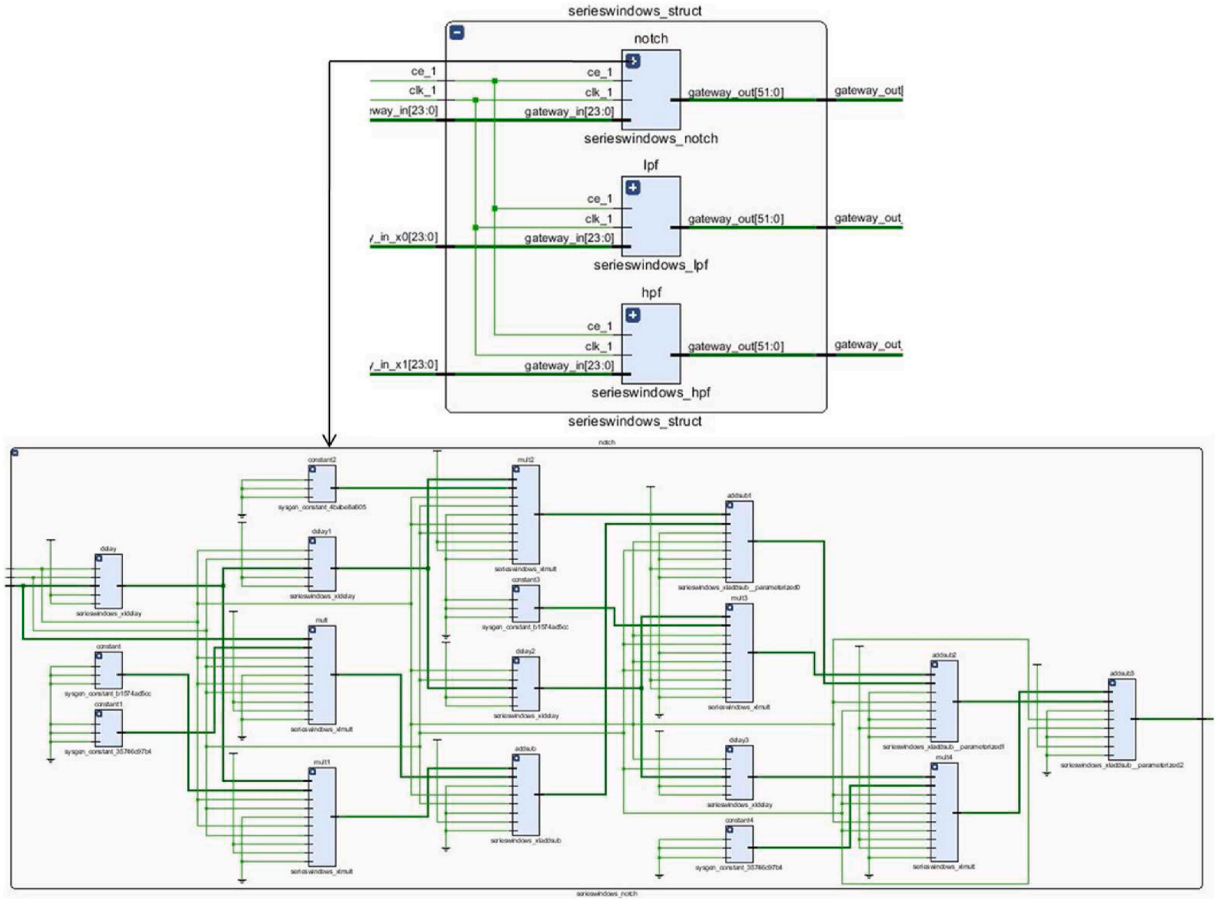

Fig. 8. RTL schematic of ECG denoising block and its core structure.

3.3. Comparison with other existing techniques

To evaluate the performance of proposed methodology the authors have also compared its best results from the existing state of art techniques present in the latest research architecture. In Table 4, different FPGA boards such as Spartan3E, Virtex 2P and Virtex 5 are utilized for the removal of different low-frequency and high-frequency noise present in the ECG. The comparison has been done on the basis of resource utilization and power consumption by the pre-processing block as illustrated in Table 4.

The authors are comparing their proposed pre-processing module with existing techniques. In our proposed technique, we are removing three types of noises EMG, BLW and PLI to eliminate the unwanted signal. Resource utilization and power consumption parameter of proposed technique are calculated and targeted on ZedBoard Zynq evaluation board and development kit. Comparison is done with recent year papers that denoise the ECG signal using XSG modeling and FPGA platform tabulated in Table 4. The comparison between recent approaches with proposed approach in terms of the type of noise removed, targeted FPGA board, resource utilization and power consumption is done. QRS detection technique proposed in Ref. [19] uses least square filtering method to remove BLW noise on Spartan-3A board but here for the comparison purpose we are targeting ZedBoard. P.C. Bhasker et al. Eliminates EMG and PLI noises separately using Kaiser window technique using Spartan 3E board [2,21]. It is interpreted from the Table 4 that proposed sequence architecture depletes only 0.76% of LUTs, 5.03% of registers and 6.7% of DSP in contrast to other existing papers. The sequence architecture also used very low on-chip power of 0.136 W only.

4. Conclusion and future scope

The work in this research article describes a consistent & efficient methodology for ECG denoising by utilizing different windowing and wavelet functions. The benefits of windows function and its ability to acquire useful information from the signal have been in focus in this research. To implement the ECG denoising block on hardware is a challenging task to attain low resource capacity and power consumption. The hardware implementation of the proposed block is done on FPGA as compared to DSP and MCU because it provides effective

Table 4
Comparison with recent existing techniques.

References	Filter design technique	Noises Removed	FPGA boards	Resource utilization (%)			Power Consumption
				LUT	Slice Register	I/O Block	On- Chip Power
Proposed	Bartlett (Sequence)	EMG, BLW PLI	ZedBoard (Zynq-7000 AP SoC)	0.76	5.03	6.7	136
[19]	Least-square approximation	BLW	Zedboard (Zynq-7000 AP SoC)	0.46	0.44	22.5	142
[20]	Kaiser	EMG	Spartan 3E (XC3S500e-4fg320)	1.19	1.67	7.32	–
[21]	Kaiser	PLI	Spartan 3E (XC3S500e-4fg320)	21	24	9	89

resourcefulness, high speed, and ease of computation for biomedical signal processing applications. In this paper, a proposed collateral and sequence methods were implemented using windows and wavelet techniques are simulated on FPGA. Among collateral and sequence architecture; sequence architecture provides better results as it acquires only 462 Slice LUTs, 894 Slice registers and only 18 DSP for symmetric Bartlett window function. The chosen architecture has consumed only 0.136 W of on-chip power. The utilization and execution speed denoted the ability to perform the transform using the proposed implementation efficiently and in real-time. For the proposed ECG denoising block the result lead to conclude only 0.76% of LUTs, 5.03% of registers and 6.7% of DSP is the resource utilization and 136 mW is on-chip power is consumed by Zedboard; which is less as compared to Virtex and Kintex FPGA board. In the future, the proposed ECG denoising block methodology is extended by the ECG feature extraction block on FPGA for the detection of various CVDs. In future, the Chosen architecture helps to design an overall expert system for the classification of several CVDs.

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Declaration of competing interest

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