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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
MAKEUP TEST EXAMINATION- April 2018
B.Tech VIth Semester

COURSE CODE: 10B11CI613 MAX. MARKS: 25
COURSE NAME: Computer Organization and Architecture
COURSE CREDITS: 4 MAX. TIME: 1.5 Hrs

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

Que 1. ***[6 Marks]*** Answer the following questions-

(a). Describe the QPI four-layer protocol architecture in detail. Also explain the multilane distribution of flits to phits with proper diagram.

(b). List and briefly define the main structural components of a computer.

(c). Explain Moore's law.

Que 2. ***[8 Marks]*** Consider the execution of a program which results in the execution of 2 million instructions on a 400-MHz processor. The program consists of four major types of instructions. The instruction mix and the CPI for each instruction type are given below based on the result of a program trace experiment:

Instruction Type	CPI	Instruction Mix
Arithmetic and Logic	1	60%
Load/Store with cache hit	2	10%
Branch	4	18%
Memory reference with cache miss	8	12%

Now, assume that the program can be executed in eight parallel tasks or threads with roughly equal number of instructions executed in each task. Execution is on an 8-core system with each core (processor) having the same performance as the single processor originally used. Coordination and synchronization between the parts adds an extra 25,000 instruction executions to each task. Assume the same instruction mix as in the table for each task, but increase the CPI for memory reference with cache miss (searched information is not available) to 12 cycles due to contention for memory.

a. Determine the average CPI.

b. Determine the corresponding MIPS rate.

c. Calculate the speedup factor.

d. Compare the actual speedup factor with the theoretical speedup factor determined by Amdhal's law.

Que 3. ***[4 Marks]*** For the 8-bit word 11000010, the check bits stored with it would be 0010. Suppose when the word is read from memory, the check bits are calculated to be 1001. What is the data word that was read from memory?

Que 4. ***[4 Marks]***Consider a 6 drive, 150 GB pen drive RAID array. What is the available data storage capacity for each of the RAID levels 0, 1, 3, 4, 5 and 6?

Que 5. ***[3 Marks]***What is DMA? What are its functions? Explain 8237A DMA Controller.