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Optimization of Drain Current and Voltage Characteristics for DP4T Double-Gate RF CMOS Switch at 45-nm Technology

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Abstract

Independent gate control in double-gate devices enhances the circuit performance and robustness while substantially reducing leakage and chip area. In this paper, we have explored the circuit techniques for a DP4T RF CMOS switch, which is an application of the independent double-gate MOSFET with symmetrical gate at 45-nm technology design and analyzed the better drain current, output voltage, ON resistance, ON/OFF ratio and insertion loss for the DP4T DG RF CMOS switch.

Keywords: 45-nm technology; Single-gate MOSFET; Double-gate MOSFET; DP4T switch; Radio frequency; RF switch; CMOS; VLSI.

1. Introduction

The enhancement in frequency response of Si-CMOS devices has motivated for their use in the millimeter and radio-frequencies wave applications, such as high capacity wireless in local area network, short-range high data-rate, wireless personal area network, and collision avoidance radar for automobiles. Using Si-CMOS for these applications allows for higher levels of integration and lower cost also improving the efficiency. Since for the 65-nm technology has application of 60 GHz power amplifier designs, but recently reported research [1] has demonstrated 60 GHz power amplifiers in 45-nm technology. Bulk MOSFETs show the severe short channel effects like drain induced barrier lowering (DIBL) and threshold voltage roll-off, as the channel length of the device goes down in nanometer range.

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Double-gate (DG) MOSFETs are good candidates to replace the conventional MOSFETs in this particular region because of their excellent immunity to short channel effects [2]. DG devices can be employed with tied gates or independently controlled gates configurations. The back-gate bias can control the threshold voltage in fully depleted silicon-on-insulator (FD/SOI) devices with thin buried oxide or in the DG devices [3]. Independent controlling of the front and back-gates provides wide design and application opportunities. The ability to enhance gate control and provide logic versatility with a tight physical image and satisfactory leakage characteristics in the DG technologies gives ample reasons to pursue research and development activities in this area.

In the present work, we investigate the electrical properties of the DG MOSFET, which turn out to be very promising for the device miniaturization below 0.1 μm. We optimize the drain current and discussed the characteristics voltage and present the comprehensive study for the effect of gates in the DP4T RF CMOS switch performance at 45-nm technology in terms of output voltage. Device structures with different gates are studied to understand the effect of device geometry on RF CMOS with single-gate (SG) MOSFET and double-gate (DG) MOSFET. The devices used in this paper are 45-nm CMOS technology. The 45-nm devices have a gate length of 40 nm and V_{DD} = 1.1 V. The output voltage observations were analyzed in the range of 0 to 5.0 ns time base. The organization of the paper is as follows: The design of DG MOSFET with the schematic is shown in the Section 2. The switching characteristics of DP4T DG RF CMOS switch are presented in the Section 3 and finally, Section 4 concludes the works and recommends the future directions.

2. Design of DG MOSFET

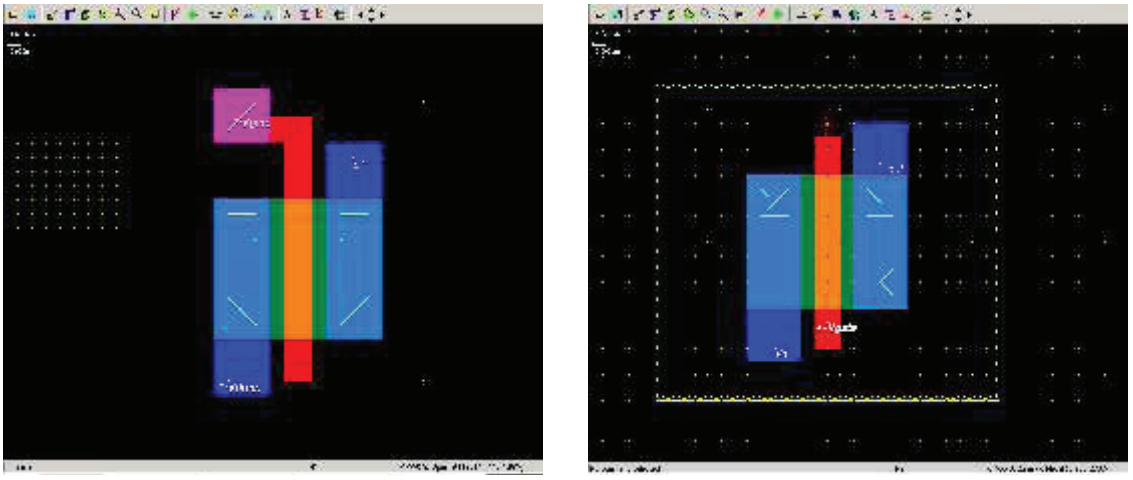
As compared with planar CMOS devices, the DG devices exhibit smaller sub threshold and gate leakage currents while offering stronger current drive. Independent biasing of the front-gate and back-gate in the DG technologies has been reported to enhance performance and reduce chip area due to the reduction of transistor count to implement a given logic functions. Separate gate access allows for simplification of circuit topologies and area compactness, both lead to power and speed improvement in addition to design flexibility [4].

In symmetrical DG devices, very high body doping density with poly-silicon gate or undoped body with near mid-gap metal gate material is used to set the desired threshold voltage (V_{th}). For an asymmetrical DG n-MOSFET, the front and back-gate typically, consists of n+ poly-silicon and p+ poly-silicon, respectively. For asymmetrical DG p-MOSFET, the opposite type of gate is applied that is p+ poly-silicon for the front gate and n+ poly-silicon for the back gate. The predominant front-channel has a significantly lower threshold voltage (V_{th}) and much larger drive current compared with the weak back-channel [5-8], which is also verified in the next sections. The front-channel can be modulated by back-gate biasing through gate-to-gate coupling. This modulation mechanism is significantly stronger than the well/body bias in bulk or partially depleted silicon-on-insulator (PD/SOI) CMOS devices.

In general for the symmetrical DG device (even n-type or p-type), the front-gate remains relatively constant with back-gate bias, as the gate to gate coupling is limited at the strong inversion charge at back surface. In the similar way for asymmetrical DG device, the modulation effect is very significant, as the gate to gate coupling is extended until the back surface becomes strongly inverted (the weak back-channel has a high, about 1.0 V higher than the front-channel). In bulk and PD/SOI devices, the effectiveness and operating frequency of the well/body bias are limited by the distributed resistance and capacitance (R and C) of the well and body contact. It also tends to degrade with technology scaling due to the lower body factor in scaled devices.

Area compactness is best understood in complex gates. The use of double-gate increases the cell area compared to that of a same width single-gate device. The advantage of realization of more complex logic, optimization of same net contact sharing, increase in drive current by controlling gates, decrease in output

voltage as the switch OFF, inter-cell wiring distance, layout compactness for larger group of front-gate devices, the significant reduction of switching capacitances are useful and motivate to use the DG MOSFET for a RF CMOS switch.



(a) (b)

Figure 1. Layout of the a) Single-Gate (SG) MOSFET and, b) Double-Gate (DG) MOSFET.

3. Switching Characteristics Of DP4T DG RF CMOS Switch

The switch is designed to be part of the microwave applications for switching system between transmitting and receiving modes. In this work, the DP4T switch has been designed to have a symmetrical structure of transmitter (Tx) and receiver (Rx) to be operated at GHz range, using 45-nm technology with a tool Microwind 3.1 version. Fig. 2 shows the schematic of the DP4T RF CMOS switch and its characteristics are shown in Fig. 3. Transistors M_1 and M_2 perform the main ON and OFF switching function, while the shunt transistor M_3 and M_4 which are cascade to M_1 and M_2 respectively are used to improve the isolation of the switch by grounding RF signals on the side which is turned OFF. The switch can also connects coupling capacitors C_1 and C_2 which allow dc biasing of the T_x and R_x nodes of the switch. The gate resistances R_1 and R_2 are implemented to improve dc isolation [9, 10].

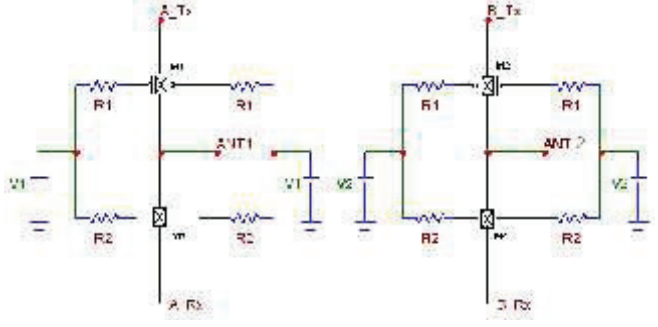


Figure 2. DP4T DG RF CMOS Transceiver Switch.

The presented compact model accounts for charge quantization within the channel, Fermi statistics, and nonstatic effects in the transport model. The main finales of this compact switch model are:

1) The DIBL is minimized by the shielding effect of the DG MOSFET, which allows reduction in the channel length from 45 nm.
2) The device transconductance per unit width is maximized by the combination of the DG MOSFET and by a strong velocity overshoot, which occurs in response to the abrupt variation of the electric field at the source end of the channel [11].
3) Increase in the device transconductance per unit width can be further strengthened near the drain in view of the short device length.

As a result, a sustained electron velocity of nearly twice the saturation velocity is achievable. The following observations proved the potential performance advantages of the DG device architecture as a switch.

A. Drain Current Analysis

The drain current is described with the idea of Pao and Sah phenomena, that includes both the drift and diffusion transport tendencies in the silicon film, resulting in a current description with flat transitions between the linear and saturation operating regions. Under the approximation that the mobility is independent of the position in the channel, the drain current ID can be expressed as [12]:

$$I_d = \mu \frac{W}{L} \int_0^{V_{ds}} Q_I dV \tag{1}$$

where μ, W, L and QI are the effective electron mobility, channel width, effective channel length, and total (integrated in the transverse direction) inversion charge density inside the silicon film of a symmetric DG MOSFET at a given location x defined by:

$$Q_I = -2q \int_0^{t_{si}} (n - n_i) dx = -2q \int_{\phi_0}^{\phi_s} \frac{n - n_i}{F} d\phi \tag{2}$$

where F is the electric field. Since there is no fixed charge in the undoped body, QI can be taken as being the total charge in the semiconductor [12]:

$$Q_I = 2\varepsilon_s F_s = -2C_0 (V_{GF} - \phi_s) \tag{3}$$

where F_s is the electric field at the surface, and the factor of two comes from the symmetry. An equivalent to the Pao and Sah's equation for the SOI MOSFET may be obtained by substituting (3) into (2), which yields the following generalized two integral formulations for the drain current [13]:

$$I_d = 2\mu \frac{W}{L} \int_0^{V_{ds}} \int_{\phi_0}^{\phi_s} \frac{qn}{F} d\phi \, dV \tag{4}$$

with $n = n_i \, e^{\beta(\phi - V)}$.

Hence, we can conclude that for the device under test, charge Q_I in the SG MOSFET is double than the DG MOSFET. So the current will be double in the SG MOSFET as compared to the DG MOSFET.

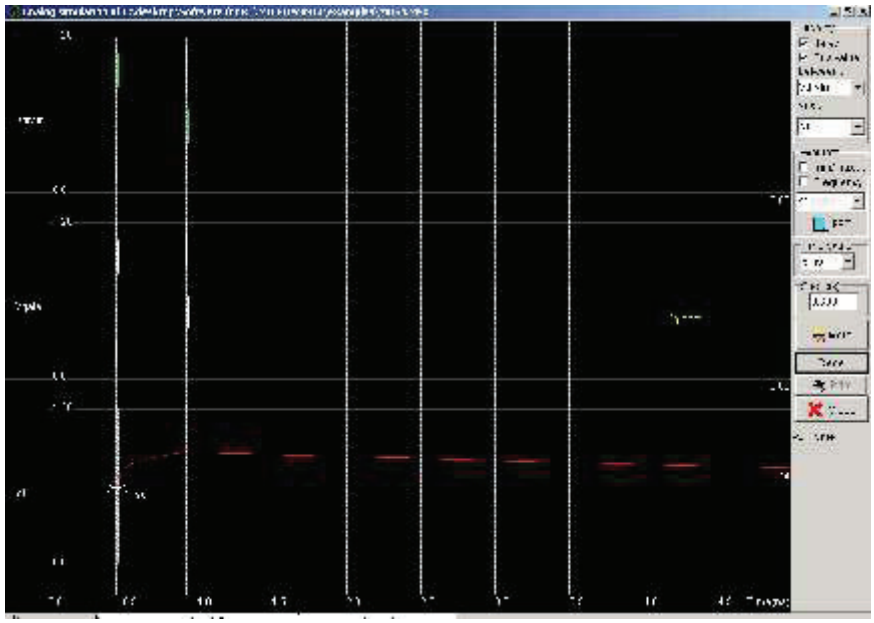
B. Voltage Characteristics

With the DP4T DG RF CMOS switch, as shown in Fig. 2, we analyzed the output voltage with respect to time as shown in Fig. 3. We present a comparative analysis of this output voltage for single-gate MOSFET (Fig. 3a) and double-gate MOSFET (Fig. 3b). For SG MOSFET, after closing the switch that is at switch OFF condition, output voltage is 0.74 V at 4.5 ns, whereas for DG MOSFET output voltage reduces to zero at 4.5 ns. This fast reduction in output voltage for the DG MOSFET device as DP4T RF CMOS switch is a better switching as compared to the SG MOSFET.

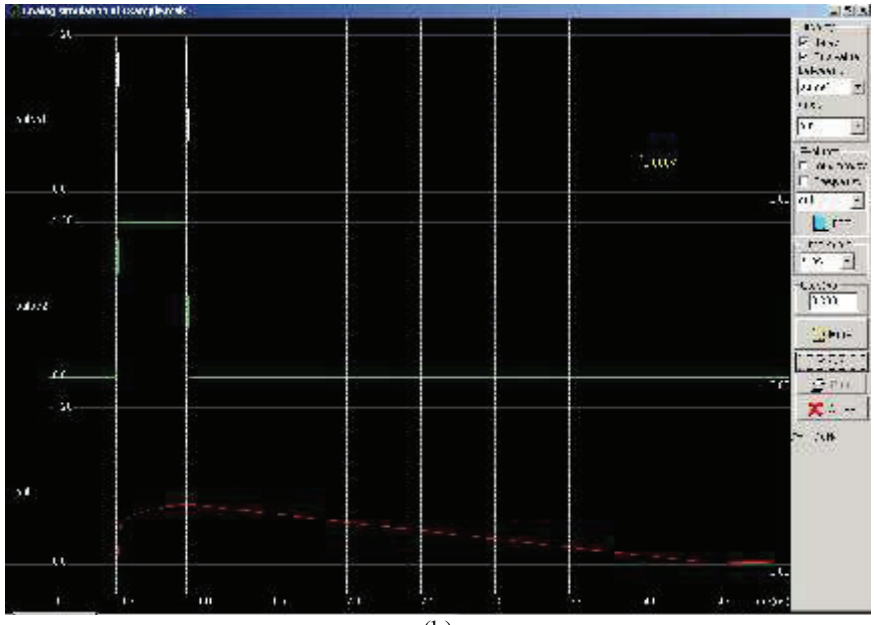
C. ON/OFF Ratio

A single switch element is characterized for on/off ratio and insertion loss. ON/OFF ratio of a single switch element is $10\log(2\pi R_{ON} C_{OFF} f_0)$ where R_{ON}, C_{OFF} and f_0 are ON resistance, OFF capacitance and

the frequency respectively. So for the DG MOSFET switch at the high frequency (GHz range) this ratio is higher, means once again switching become fast for DP4T DG RF CMOS switch.



(a)



(b)

Figure 3. Characteristic curve for a) SG n-MOSFET, and b) DG n-MOSFET.

D. Insertion Loss

The insertion loss is given by

$$\left(\frac{R_{ON} + 2Z_0}{2Z_0} \right) \tag{5}$$

where Z_0 is a fixed characteristic impedance and taken as 50 Ω. R_{ON} is the resistance of device at ON state. For DG MOSFET R_{ON} becomes $R_{ON}/2$ (parallel combination of R_{ON} due to front-gate and back-gate). So the insertion loss for the DP4T DG RF CMOS switch becomes less as compared to SG MOSFET devices.

4. Conclusions and Future Scope

In this paper we discussed the dependence of front-gate potential on the channel thickness, doping concentration, drain current, output voltage, ON/OFF ratio and insertion loss. Similarly dependence of back-gate potential can also be discussed. Moreover an analytic threshold voltage model is presented for the SG MOSFET and DG MOSFET. Device simulation is also done using a Microwind 3.1 version simulator and the results obtained are compared with the theoretical analysis for the model. The modelling results are found to be a comparative good agreement with the simulated data. The model can further be extended to obtain the drain current characteristics and the output characteristics with different materials as Hafnium (Hf) in place of silicon [14, 15].

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