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Voltage Mode Cascadable All-Pass Sections Using Single Active Element and Grounded Passive Components

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Abstract

In this paper, four new first order voltage mode cascadable all-pass sections are proposed using single active element and three grounded passive components, ideal for IC implementation. The active element used is a fully differential current conveyor. All the proposed circuit possess high input and low output impedance feature which is a desirable feature for voltage-mode circuits. Non-ideality aspects and parasitic effects are also given. As an application, a multiphase oscillator is designed. The proposed circuits are verified through PSPICE simulation results using TSMC 0.35 μm CMOS parameters.

Keywords: Analogue Signal Processing, All-Pass Filter, Current Conveyor, Voltage-Mode

1. Introduction

Voltage mode (VM) active filters with high-input and low-output impedance are of great interest because several cells of this kind can be directly connected in cascade within voltage-mode systems without additional voltage buffers. On the other hand, the use of grounded capacitor is beneficial from the point of integrated circuit implementation and also having less parasitic compared to floating counterparts [1].

First order all-pass filters are an important class of analogue signal processing circuits which have been extensively researched in the technical literature [2,3] due to their utility in communication and instrumentation systems, for instance as a phase equalizer, phase shifter or for realizing quadrature oscillators band pass filters etc. Numerous first-order voltage-mode all-pass sections (VM-APSs) employing different types of active element such as current conveyors and its different variations have been reported in the literature [4-24]. Among the cited references, several VM-APSs employ a single standard current conveyor [6-16,19-22]. Such circuits aim at realizing the first order all-pass function using optimum number of passive components, rather using grounded components or offering high input and low output impedance feature together. The circuits reported in [17,18] enjoy high input impedance but uses two active element and three grounded passive components. Some of the circuits described in [15,21-23] fall in the separate category of tunable, resistorless realizations, the most recent of these [22,23] enjoys high input and/or low output impedance. A recent published all-pass filter circuit in [24] employ two DVCCs and two passive components with the advantage of high input impedance and low output impedance, which is ideal for cascading, but it still suffer from floating resistor. But a careful survey reveals that none of the reported works realizes a VM-APS using single active element, grounded passive components, and also providing high input impedance and low output impedance features simultaneously.

This paper proposes four new first order VM cascadable all-pass sections, with high input and low output impedance using single active element and three grounded passive components, which are ideal for IC implementation. Each circuit employs two grounded resistors and one grounded capacitor. The proposed circuits are based on fully differential second generation current conveyor (FDCCII), an active element to improve the dynamic range in mixed mode application, where fully differential signal processing is required [25]. As an application, the

proposed circuit realizes a multiphase oscillator. PSPICE simulation results using TSMC 0.35 μm CMOS parameters are given to validate the circuits.

The paper is organized as follows: in Section 2, the proposed all-pass filters using FDCCII are presented. In Section 3, parasitic and non-ideal analyses of the proposed circuits are given. In Section 4, to verify the theoretical study the first order all-pass filters were constructed and simulated with PSPICE program. In Section 5, a multi- phase oscillator is implemented to show the usefulness of the proposed circuits as an illustrating example and finally the conclusion in Section 6.

2. Proposed Circuit

The FDCCII is an eight terminal analog building block with a describing matrix equation of the form [25]

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Y4} \\ V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{X+} \\ I_{X-} \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (1)$$

The symbol and CMOS implementation of FDCCII are shown in **Figure 1** [25]. The Y_1, Y_2, Y_3, and Y_4 terminals are high-impedance terminals, while X+ and X– terminals are low-impedance ones. The Z+ and Z– terminals are high impedance nodes suitable for current outputs. FDCCII is a useful and versatile active element for analog signal processing. The applications of FDCCIIs in filters and oscillators design using only grounded passive components were demonstrated in [26,27].

The voltage transfer function of an all-pass filter can be given as

$$\frac{V_{OUT}}{V_{IN}} = K\frac{s\tau - 1}{s\tau - 1} \quad (2)$$

where K is the gain constant and its sign determines whether phase shifting is from 0° to -180° or from 180° to 0°, and τ is the time constant. The four proposed first order VM cascadable all-pass sections using a single FDCCII and three grounded passive components are shown in **Figures 2(a)-2(d)**. The four circuits in **Figures 2 (a)-2(d)** are characterized by the voltage transfer function as

$$\frac{V_{OUT}}{V_{IN}} = K\left(\frac{s-(1/C_1)[(1/R_2)-(1/R_1)]}{s+(1/R_1C_1)}\right) \quad (3)$$

For $R_2 = R_1/2$ Equation (3) becomes

$$\frac{V_{OUT}}{V_{IN}} = K\frac{sR_1C_1 - 1}{sR_1C_1 + 1} \quad (4)$$

where the value of K = +1 for Circuit-I and Circuit-II (**Figures 2(a)** and **2(b)**) and the value of K = –1 for Circuit-III and Circuit-IV (**Figures 2 (c)** and 2**(d)**).

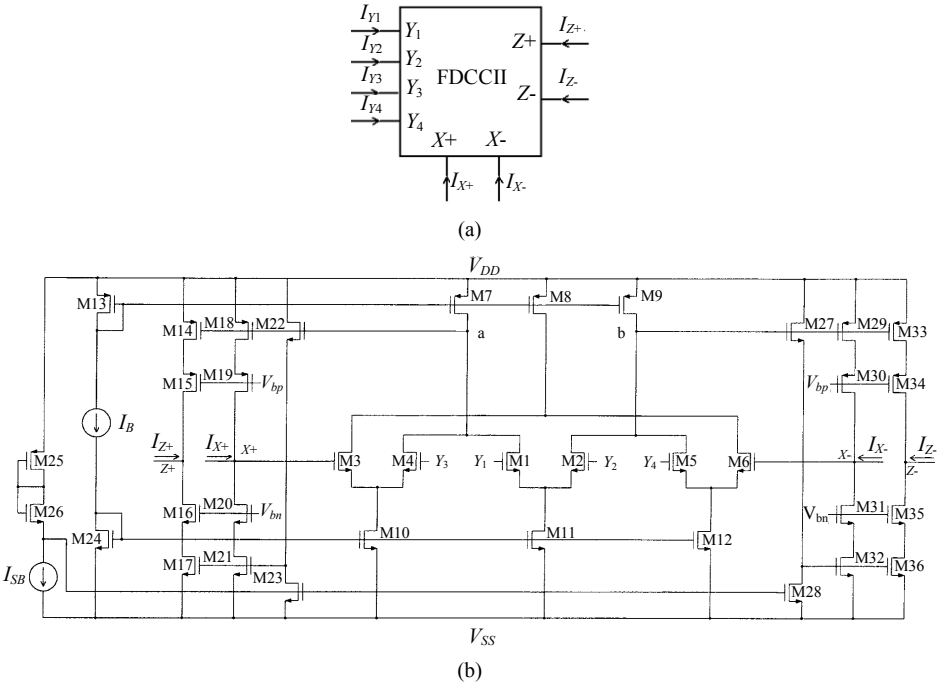

Figure 1. Fully differential second generation current conveyor (a) symbol (b) CMOS implementation [25].

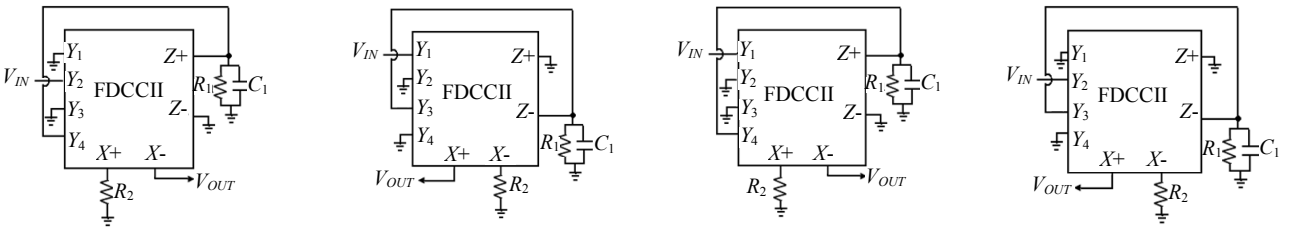

Figure 2. Proposed first order cascadable all-pass filters (a) circuit-I; (b) circuit-II; (c) circuit-III and (d) circuit-IV.

The salient features of the four proposed circuits are high input and low output impedance, single active element and use of grounded passive components; the three features are not exhibited together in any of the available works, including the most recent circuits [4-24]. It may be noted that the new circuits are based on a topology with input at *Y* and output at one of the *X* terminals, the other *X*-terminal being terminated by a resistor. The four proposed circuits with similar properties being derivable from a topology are a result of the versatility of FDCCII.

It is also worth mentioning that four additional new circuits can further be obtained from the proposed circuits by replacing the resistor (R_2) with a capacitor (C_2). However these circuits would employ a capacitor at *X* terminal, thus degrading high frequency operation. This aspect will not be further elaborated for brevity reasons.

3. Parasitic and Non-Ideal Analysis

3.1. Parasitic Effects

A study is next carried out on the effects of various parasitic of the FDCCII used in the proposed circuits. These are port *Z* parasitic in form of $R_Z//C_Z$, port *Y* parasitic in form of $R_Y//C_Y$ and port *X* parasitic in form of series resistance R_X [13]. The proposed circuits are reanalyzed taking into account the above parasitic effects. The voltage transfer function (assuming $R << R_Y$ or R_Z and $R_X << R$), for the circuits of **Figures 2(a)-2(d)**, is given as

$$\frac{V_{OUT}}{V_{IN}} = K\left(\frac{s-(1/(C_1+C_P))[(1/R')-(1/R_1)]}{s+(1/R_1(C_1+C_P))}\right) \qquad (5)$$

where, $R' = R_2 + R_X$, (for **Figures 2(a)-2(d)**), $K = +1$, (for **Figures 2(a)** and **2(b)**), $K = -1$, (for **Figures 2(c)** and **2(d)**), and $C_P = C_{Z+} + C_{Y4}$ (for **Figures 2(a)** and **2(c)**), and $C_P = C_{Z-} + C_{Y3}$ (for **Figures 2(b)** and **2(d)**).

From (5), it is seen that the gain is unity and the pole-frequency is

$$\omega_o = \frac{1}{R_1(C_1+C_P)} \qquad (6)$$

From (5), the parasitic resistance/capacitances merge with the external value. Such a merger does cause slight deviation in circuit's parameters, which can be eliminated by pre-distorting the element values to be used in the circuit. It is seen that the pole-frequency would be slightly deviated (in deficit) due to these parasitics. The deviation is expected to be small for an integrated FDCCII; the actual value would be given in the 'simulation results'.

3.2. Non-Ideal Analysis

Taking the non-idealities of the FDCCII into account, the relationship of the terminal voltages and currents can be rewritten as

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Y4} \\ V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & \beta_3 & 0 & 0 & 0 & 0 & 0 \\ -\beta_4 & \beta_5 & 0 & \beta_6 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \alpha_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \alpha_2 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{X+} \\ I_{X-} \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \qquad (7)$$

where α_i (i = 1, 2) accounts for current transfer gains and β_i (i = 1, 2, 3, 4, 5, 6) accounts for voltage transfer gains of the FDCCII. These transfer gains differ from unity by the voltage and current tracking errors of the FDCCII. More specifically, $\alpha_i = 1 - \delta_i$, ($|\delta_i| << 1$) δ_1 is the current tracking error from *X*+ to *Z*+ and δ_2 is the current tracking error from *X*– to *Z*–. Similarly, $\beta_i = 1 - \varepsilon_i$, ($|\varepsilon_i| << 1$) where, voltage tracking errors are ε_1 (from Y_1 to *X*+), ε_2 (from Y_2 to *X*+), ε_3 (from Y_3 to *X*+), ε_4 (from Y_1 to *X*–), ε_5 (from Y_2 to *X*–), and ε_6 (from Y_4 to *X*–). The circuits of **Figures 2(a)-2(d)** are reanalyzed using (7) and the non-ideal voltage transfer functions are found as

Circuit-I:

$$\frac{V_{OUT}}{V_{IN}} = \beta_5\left(\frac{s-[(\alpha_1\beta_2\beta_6R_1-\beta_5R_2)/\beta_5C_1R_1R_2]}{s+(1/C_1R_1)}\right) \qquad (8)$$

Circuit-II:

$$\frac{V_{OUT}}{V_{IN}} = \beta_1 \left(\frac{s - [(\alpha_2\beta_3\beta_4 R_1 - \beta_1 R_2)/\beta_1 C_1 R_1 R_2]}{s + (1/C_1 R_1)} \right) \quad (9)$$

Circuit-III:

$$\frac{V_{OUT}}{V_{IN}} = -\beta_4 \left(\frac{s - [(\alpha_1\beta_1\beta_6 R_1 - \beta_4 R_2)/\beta_4 C_1 R_1 R_2]}{s + (1/C_1 R_1)} \right) (10)$$

Circuit-IV:

$$\frac{V_{OUT}}{V_{IN}} = -\beta_2 \left(\frac{s - [(\alpha_2\beta_3\beta_5 R_1 - \beta_2 R_2)/\beta_2 C_1 R_1 R_2]}{s + (1/C_1 R_1)} \right) (11)$$

From (8)-(11), it is seen that the pole-frequency is unaltered by FDCCII non-idealities for all the transfer functions of the respective circuit, but the filters gain are slightly modified due to the FDCCII non-idealities. Thus the pole-frequency sensitivity to the FDCCII nonidealities is zero, and the filters gain sensitivity to these non-idealities is found within unity in magnitude. This suggests a good sensitivity performance for the proposed circuits.

4. Simulation Results

To verify theoretical result the proposed filter circuits were simulated by the PSPICE simulation program. The FDCCII was realized based on the CMOS implementation as shown in **Figure 1** [25] and simulated using TSMC 0.35 μm, level 3 MOSFET parameters as listed in **Table 1**. The aspect ratio of the MOS transistors are listed in **Table 2**, with the following DC biasing levels V_{dd} = $-V_{ss}$ = 3.3 V, V_{bp} = V_{bn} = 0 V, and I_B = I_{SB} = 1.7 mA. The circuit-I (**Figure 2(a)**) was designed with C_1 = 50 pF, R_1 = 2 kΩ and R_2 = 1 kΩ. The theoretical designed pole frequency was 1.59 MHz. The phase and gain plots are shown in **Figure 3**. The phase is found to vary with frequency from 180° to 0° with a value of 90° at the pole frequency, and the pole frequency was found to be 1.54 MHz, which is close to the theoretical value. The circuit was next used as a phase shifter introducing 90° shift to a sinusoidal voltage input of 1 Volt peak at 1.59 MHz. The input and output waveforms are given in **Figure 4** which verify the circuit as a phase shifter. The THD variation at the output for varying signal amplitude at 1.59 MHz was also studied and the results shown in **Figure 5**. The THD for a wide signal amplitude (few mV-1V) variation is found within 4.27% at 1.59 MHz. The Fourier spectrum of the output signal, showing a high selectivity for the applied signal frequency (1.59 MHz) is also shown in **Figure 6**. Both theoretical and simulated pole frequencies are found to closely match; the discrepancy (deficit) in simulated frequency being the result of various parasitic discussed in Section 3.

Table 1. 0.35 μm level 3 MOSFET parameters.

NMOS:
LEVEL = 3 TOX = 7.9E – 9 NSUB = 1E17
GAMMA = 0.5827871 PHI = 0.7 VTO = 0.5445549 DELTA = 0
UO = 436.256147 ETA = 0 THETA = 0.1749684
KP = 2.055786E – 4 VMAX = 8.309444E4 KAPPA=0.2574081
RSH = 0.0559398 NFS = 1E12 TPG = 1 XJ = 3E – 7
LD = 3.162278E – 11 WD = 7.04672E – 8 CGDO = 2.82E – 10
CGSO = 2.82E – 10 CGBO = 1E – 10 CJ = 1E – 3 PB = 0.9758533
MJ = 0.3448504 CJSW = 3.777852E – 10 MJSW = 0.3508721
PMOS:
LEVEL = 3 TOX = 7.9E – 9 NSUB = 1E17
GAMMA = 0.4083894 PHI = 0.7 VTO = –0.7140674
DELTA = 0 UO = 212.2319801 ETA = 9.999762E – 4
THETA = 0.2020774 KP = 6.733755E – 5 VMAX = 1.181551E5
KAPPA = 1.5 RSH = 30.0712458 NFS = 1E12 TPG = –1
XJ = 2E – 7 LD = 5.000001E – 13 WD = 1.249872E – 7
CGDO = 3.09E – 10 CGSO = 3.09E – 10 CGBO = 1E – 10
CJ = 1.419508E – 3 PB = 0.8152753 MJ = 0.5
CJSW = 4.813504E – 10 MJSW = 0.5

Table 2. Transistor aspect ratios for the circuit shown in Figure 1.

Transistors	W(μm)	L(μm)
M1-M6	60	4.8
M7-M9, M13	480	4.8
M10-M12, M24	120	4.8
M14,M15,M18,M19,M25,M29,M30,M33,M34	240	2.4
M16,M17,M20,M21,M26,M31,M32,M35,M36	60	2.4
M22,M23,M27,M28	4.8	4.8

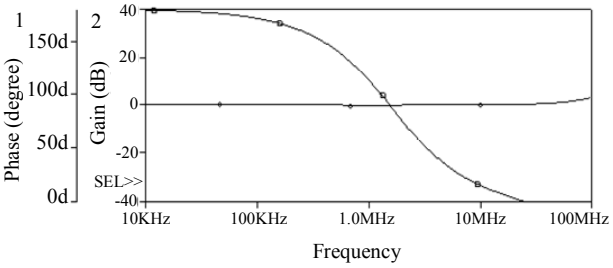

Figure 3. Gain and phase responses for the circuit-I.

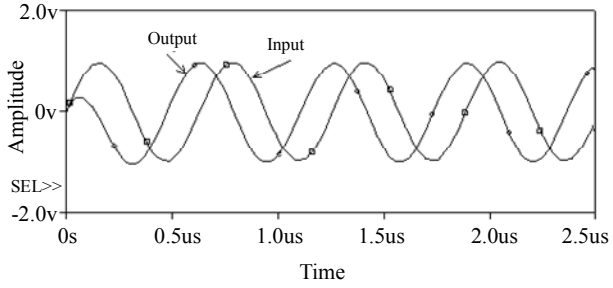

Figure 4. Input/output waveshapes for Circuit-I at 1.59 MHz.

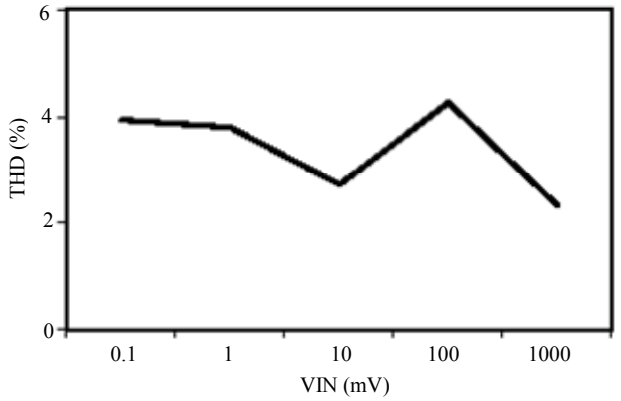

Figure 5. THD variation at output with signal amplitude at 1.59 MHz.

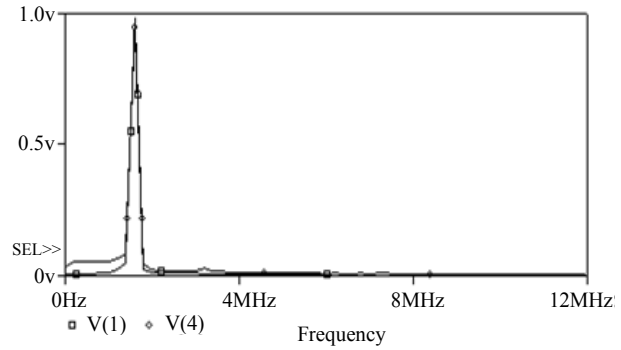

Figure 6. Fourier spectrum of Input-output signal at 1.59 MHz.

Similarly, the circuit-III (**Figure 2(c)**) was designed with the same values and frequency as above. The phase and gain plots are shown in **Figure 7**. The phase is found to vary with frequency from 0 to –180° with a value of –90° at the pole frequency, and the pole frequency was found to be 1.54 MHz, which is close to the theoretical value. The circuit was next used as a phase shifter introducing –90° shift to a sinusoidal voltage input of 1 Volt peak at 1.59 MHz. The input and output waveforms are given in **Figure 8** which verify the circuit as a phase shifter.

5. Application Example

To further illustrate the utility of the proposed circuits a sinusoidal oscillator producing a number of quadrature signals was realized using the Circuit-I (**Figure 2(a)**). By connecting Y_2 terminal, the input node to the *Z*-terminal of FDCCII, connecting resistor (R') and capacitor (C') at *X*– and *Z*– terminals of FDCCII. The resulting circuit is shown in **Figure 9**. The circuit analysis yields the following characteristic equation

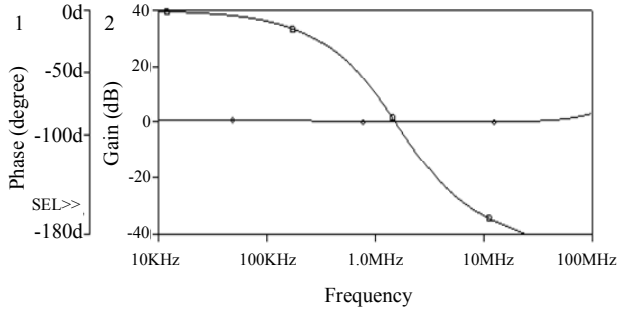

Figure 7. Gain and phase responses for the circuit-III.

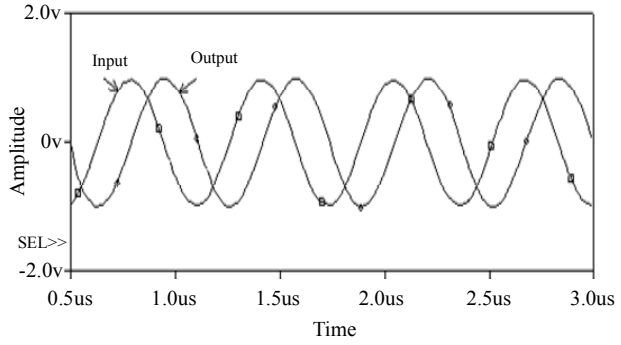

Figure 8. Input/output waveshapes for Circuit-III at 1.59 MHz.

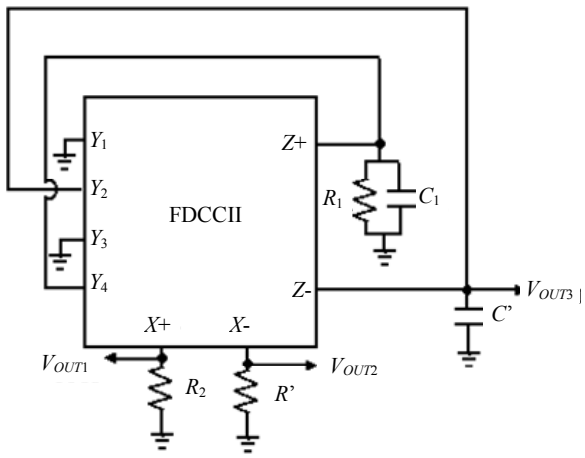

Figure 9. Multiphase oscillator using Circuit-I of Figure 2(a).

$$s^2 + s\left[\frac{1}{C_1R_1} - \frac{1}{C'R'}\right] + \frac{R_1 - R_2}{C_1C'R_1R_2R'} = 0 \qquad (12)$$

At the frequency of oscillation, with $s = j\omega$, the Equation (5) gives the frequency of oscillation (*FO*) and condition of oscillation (*CO*) as

$$FO: \omega_o = \sqrt{\frac{R_1 - R_2}{C_1C'R_1R_2R'}}\ ;\ CO:\ C'R' \geq C_1R_1 \qquad (13)$$

Assuming $R' = R_1 = 2R_2$; $C' = C_1$

$$FO: \omega_o = \frac{1}{2C'R'} \quad (14)$$

From **Figure 9**, at oscillating frequency the circuit provides three quadrature voltage outputs (V_{OUT1}, V_{OUT2} and V_{OUT3}) whose phasor relationship is shown in **Figure 10**.

The circuit was designed with $C_1 = C' = 50$ pF, $R_1 = R' = 2$ kΩ, and $R_2 = 1$ kΩ, the theoretical frequency of oscillation was around $f_o = 1.59$ MHz, whereas the simulated values as found from the result was $f_o = 1.54$ MHz. The quadrature oscillations are shown in **Figure 11**.

6. Conclusions

This paper has presented four new first-order VM cascadable all-pass sections, each employing single FDCCII, two resistors and one capacitor. The salient features of all the proposed circuits are high input and low output impedance, single active element and use of grounded passive components. The proposed circuits with grounded components in each case are suited for IC implementation in CMOS technology. Non-ideality aspects and parasitic effects are also studied. The circuits are verified through PSPICE simulations using TSMC 0.35 µm CMOS parameters. Application example in the form of multiphase oscillator is also given and also verified with good results. The proposed circuits are ideal for voltage-mode applications as well as good for IC implementation, making them a future prospect for integration.

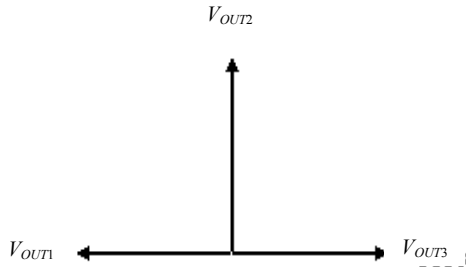

Figure 10. Phasor diagram of multiphase oscillator.

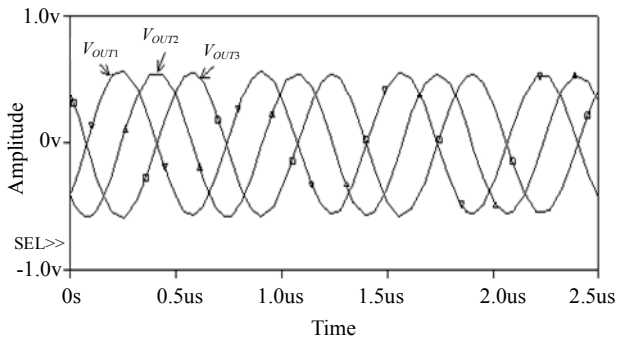

Figure 11. Quadrature voltage outputs of multiphase oscillator.

7. Acknowledgements

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