JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- FEB-2023

COURSE CODE (CREDITS): 18B11EC612 (3) MAX. MARKS: 15

COURSE NAME: VLSI Technology

COURSE INSTRUCTORS: Dr. Harsh Sohal MAX. TIME: 1 Hour

Note: *All questions are compulsory. Marks are indicated against each question in square brackets.*

Q1. [CO2][6]

(a) What is Moore's Law? Give different definitions available. Is it applicable to microprocessors? Has the die size ever played a role in Moore's law with respect to Microprocessors? [3]

(b) What is Technology scaling in VLSI? What is the need of efficient design methods at various levels of abstraction? Explain various levels of abstraction and their importance in modern VLSI design. [1+1+1]

Q2. [CO1+CO2][6]

(a) Explain various Fundamental Design Metrics in VLSI Design [2]

(b) You are given a wafer of the size of 30 cm, die size of 2.5 cm^2, with 1 defects/cm^2; α (the measure of manufacturing process complexity)=3. Cost of the wafer is INR 200,000. Calculate: (i) dies per wafer (ii) die yield (iii) cost of one die. [1+1+2]

Q3. [CO1+CO2] [3]

(a) Describe the following with respect to VLSI circuits: [0.5×4=2]

(i) Fan Out

(ii) Noise Immunity

(iii) Cross talk

(iv) Feature size.

(b) For a given inverter the V_{OH}=1.9V; V_{OL}= 0.2V; V_{IL} = 0.4V; V_{IH}=1.7V. Calculate Noise Margins, NM_L and NM_H. [1]