JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATIONS-2023

M.Tech-II Semester (ECE)

COURSE CODE (CREDITS): 21M11EC211 (3) MAX. MARKS: 15

COURSE NAME: Digital System Design using Verilog HDL .

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 1 Hour

Note: All questions are compulsory. Marks are indicated against each question in square brackets.

Q1. When Pascal, FORTRAN, and C languages were being used, why did Hardware Description Languages (HDLs) emerge? Discuss in detail. **[CO-1, 2 marks]**

Q2. What are the two basic methodologies available for digital design? Discuss with the help of a suitable example. **[CO-1, 2 marks]**

Q3. What do instance and instantiation signify in Verilog HDL? Support your answer with a suitable example. **[CO-1, 2 marks]**

Q4. Hardware Description Languages (HDLs) offer many advantages over traditional schematic-based design. Justify this statement with suitable points. **[CO-1, 2 marks]**

Q5. What are the four levels of abstraction using which the internals of module can be written in Verilog HDL? Discuss with brief description of each. **[CO-1, 2 marks]**

Q6. A digital circuit for 4-bit Ripple Carry Counter has to be designed. Write a program (design block and stimulus block) in Verilog HDL to design it. **[CO-2, 3 marks]**

Q7(i). Discuss with justification about legal/illegal comments in Verilog HDL out of the following:

a) /* c= a xor b; /* d=~e; */ f=g &&h; */
b) z= x or y // or operator on 2 operands **[CO-2, 0.5*2=1 mark]**

Q7(ii).

a) Is Verilog HDL a case sensitive language? How are keywords written in this?
b) For modeling of real digital circuits, symbol X is very important. What does it signify in Verilog HDL? **[CO-2, 0.5*2=1 mark]**