Navean Jaglan

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- May 2018

B.Tech 4th Semester

COURSE CODE: 10B11EC401

COURSE NAME: Digital Electronics

COURSE CREDITS: 4

MAX. MARKS: 35

MAX. TIME: Two Hrs

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

1. A clocked Sequential circuit is provided with a single input X and a single output Z. Whenever the input produces a string of pulses 111 or 000 and at the end of sequence it produces an output Z = 1 and overlapping is also allowed.
   (a) Obtain the state diagram
   (b) Obtain the state table.
   (c) Design the sequence detector.

   [5 Marks, CO-6]

2. Design the following:
   (a) Dual slope Integrating type ADC. [3Marks,CO-3,4]
   (b) 4-Bit Synchronous series carry Up/Down counter. [2Marks, CO-3]

3. Design a type D counter that goes through states 0,1,2,4,0,……The undesired states must always go to zero on next clock pulse.

   [5 Marks,CO-5]

4. What are the differences between synchronous and asynchronous counters? Design asynchronous BCD counter. Explain decoding errors in this counter. [5Marks,CO-3]

5. Convert D Flip Flop into SR Flip Flop.

   [4 Marks,CO-3]

6. Implement the expression F (A, B, C) = $\sum$ m (1, 2, 3, 5, 7) using 4:1 mux considering B, C as select lines.

   [3Marks,CO-1]

7. What are the advantages of 2's complement over 1's Complement. Perform the following subtraction using 2's complement 0011.1001-0001.1110. Convert the result into decimal number.

   [3Marks,CO-1,2]

8. Design BCD adder. What are the advantages of look ahead carry adder over parallel adder.

   [5 Marks,CO-4]